

Accurate On-Chip Capacitance Ratio Measurement Technique Using a Switched-Capacitor Filter

Introduction

Applications in which capacitance matching is critical:

- Switched-capacitor filters, A/D, D/A and DC/DC converters.

Capacitance ratio error sources in CMOS ICs:

- Systematic errors;
- Process gradients (t_{ox});
- Mismatches.

Techniques to improve capacitance ratio accuracy:

- Capacitors with the same area/perimeter ratio;
- Parallel connections of unit capacitors to realize each capacitance;
- Arrange unit capacitor arrays in common centroid geometry;
- Careful routing inside the capacitor array.

The Allpass Filter

A transfer function $A(z)$ whose frequency response magnitude is constant, for example,

$$|A(e^{j\omega})| = 1, \quad \text{for all } \omega$$

is called an *allpass transfer function*.

A circuit or system that has this property is an allpass “filter”.

The Allpass Filter

N^{th} -order allpass transfer function:

$$A(z) = \frac{a_N + a_{N-1}z^{-1} + \dots + a_1z^{-N+1} + z^{-N}}{1 + a_1z^{-1} + \dots + a_{N-1}z^{-N+1} + a_Nz^{-N}}$$

Can be expressed in the general form

$$A(z) = \frac{z^{-N}D(z^{-1})}{D(z)}$$

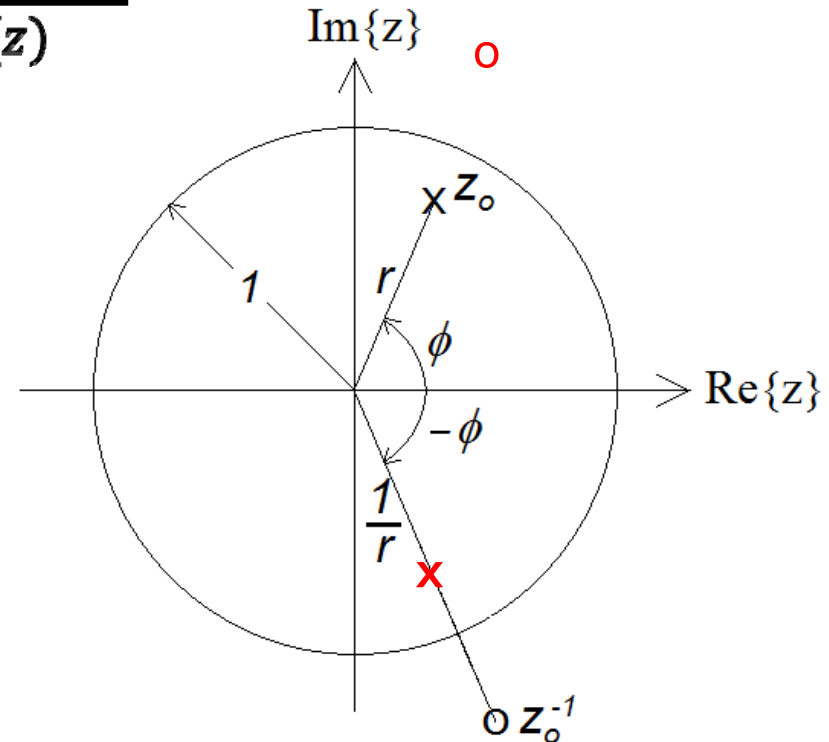
(i) If $z_o = (r)e^{j\phi}$ is a pole of $A(z)$:

$\Rightarrow z_o^{-1} = (1/r)e^{-j\phi}$ is a zero of $A(z)$

(ii) If the coefficients of $A(z)$ are real:

$\Rightarrow (z_o)^* = (r)e^{-j\phi}$ is a pole of $A(z)$

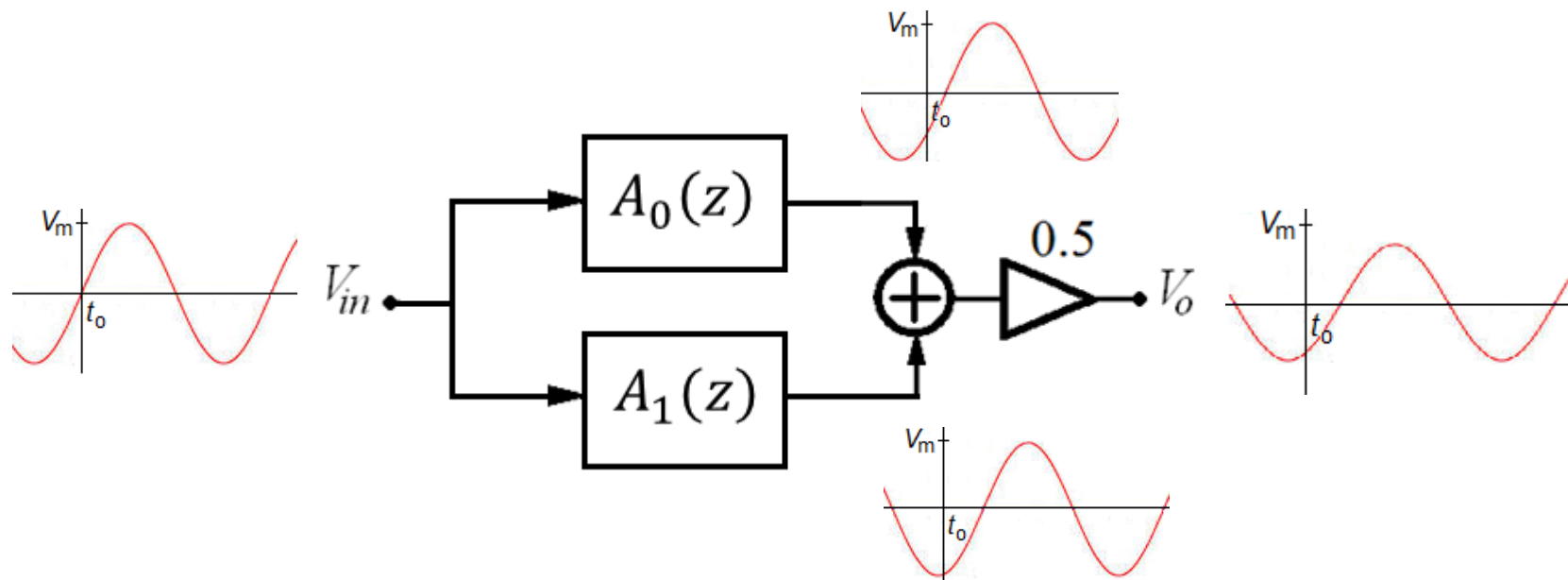
$\Rightarrow (z_o^{-1})^* = (1/r)e^{j\phi}$ is a zero of $A(z)$



The Allpass Filter

Classical transfer functions (Butterworth, Chebyshev and elliptic) of odd degree can be decomposed as:

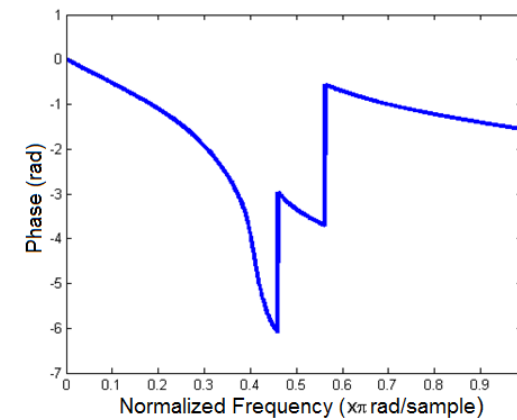
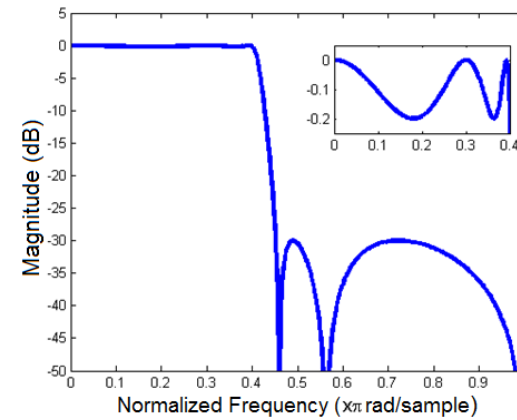
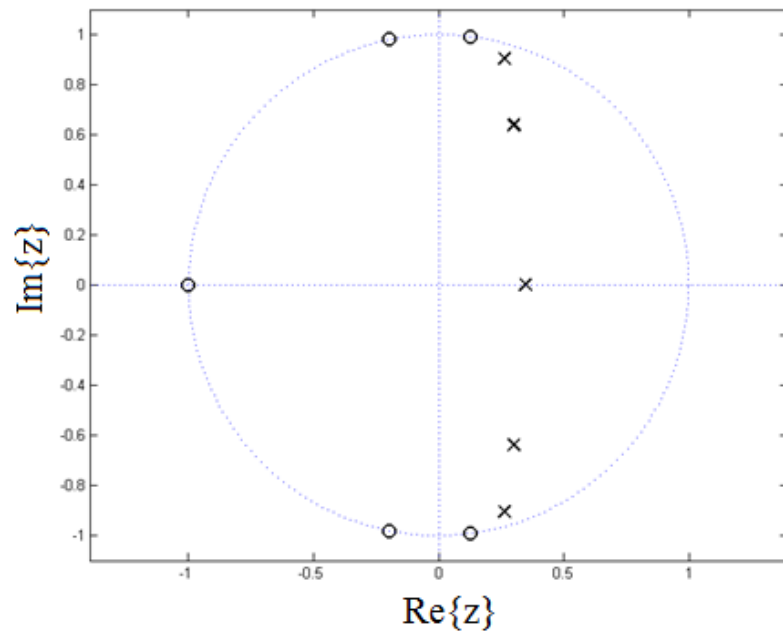
$$H(z) = \frac{1}{2} \{A_0(z) + A_1(z)\}$$



Decomposition in Allpass Sections

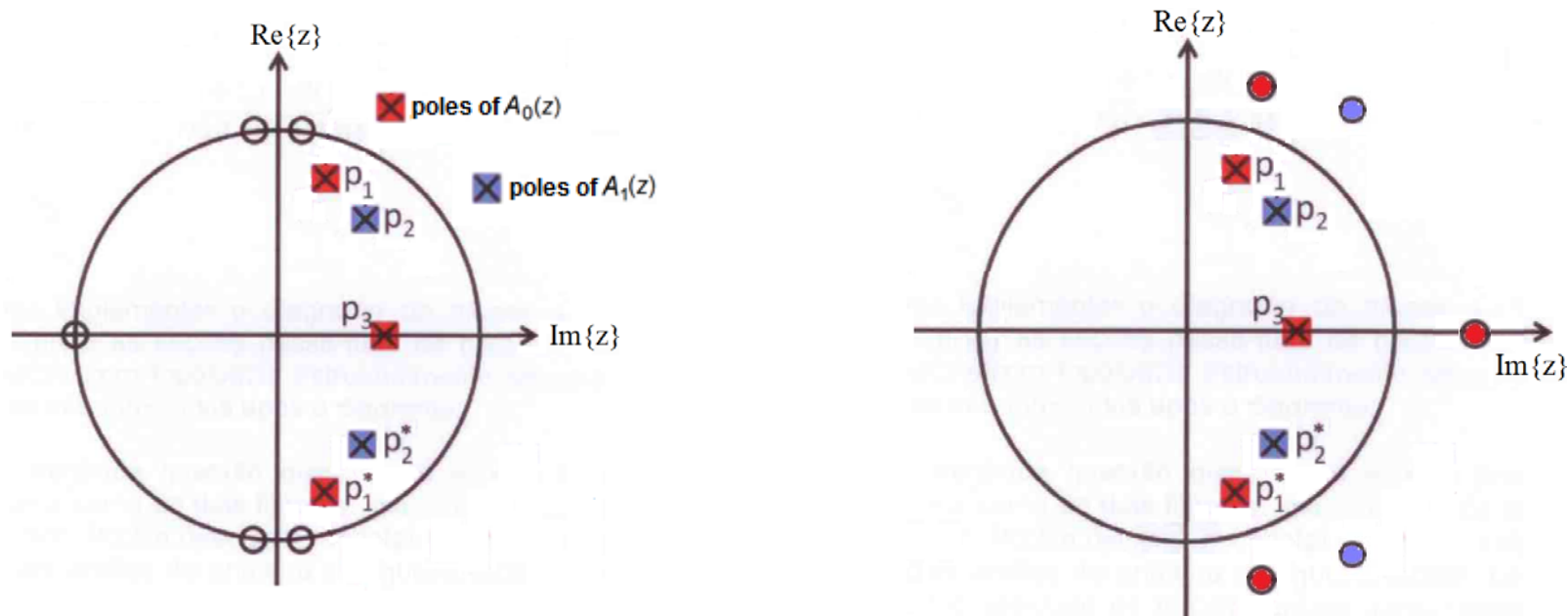
Ex.: 5th order elliptic lowpass filter:

$$f_s = 18 \text{ kHz}; f_p = 3.6 \text{ kHz}; f_r = 4.5 \text{ MHz}; r_p \leq 0.2 \text{ dB}; A_r \geq 30 \text{ dB}.$$



Decomposition in Allpass Sections

Pole interlacing property: a simple approach to identify the poles of $A_0(z)$ and $A_1(z)$:



5th order elliptic lowpass filter

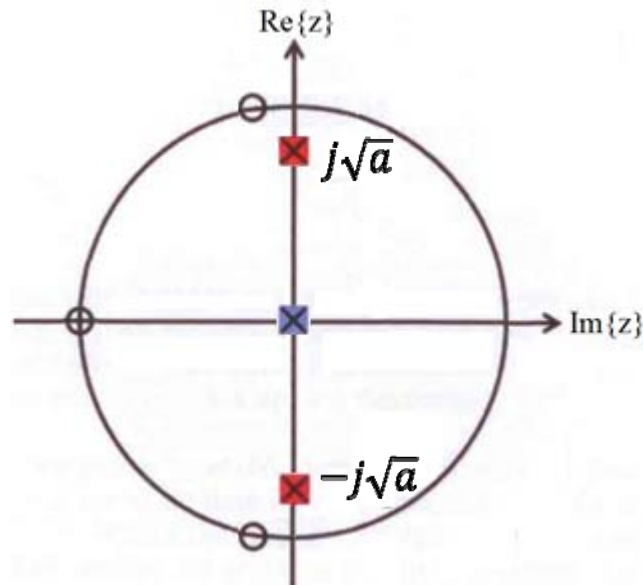
$f_s = 18\text{kHz}$; $f_p = 3.6\text{kHz}$; $f_r = 4.5\text{kHz}$;
 $r_p \leq 0.2 \text{ dB}$; $A_r \geq 30 \text{ dB}$.

$$A_0(z) = \frac{-0.308 + 1.068z^{-1} - 0.872z^{-2} + z^{-3}}{1 - 0.872z^{-1} + 1.068z^{-2} - 0.308z^{-3}}$$

$$A_1(z) = \frac{0.499 - 0.600z^{-1} + z^{-2}}{1 - 0.600z^{-1} + 0.499z^{-2}}$$

Capacitance Ratio Measurement Technique

Let us consider a 3rd order lowpass elliptic filter, whose poles are on the imaginary axis:



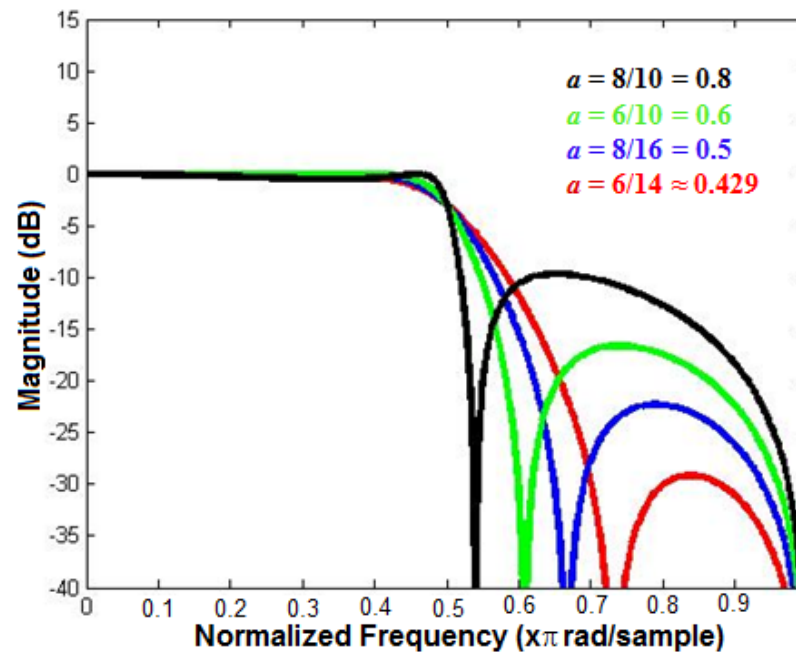
In this case:

$$A_o(z) = \frac{a + z^{-2}}{1 + az^{-2}} ; \quad A_1(z) = z^{-1} \quad \Rightarrow \quad H(z) = \frac{1}{2} \left(\frac{a + z^{-2}}{1 + az^{-2}} + z^{-1} \right)$$

Capacitance Ratio Measurement Technique

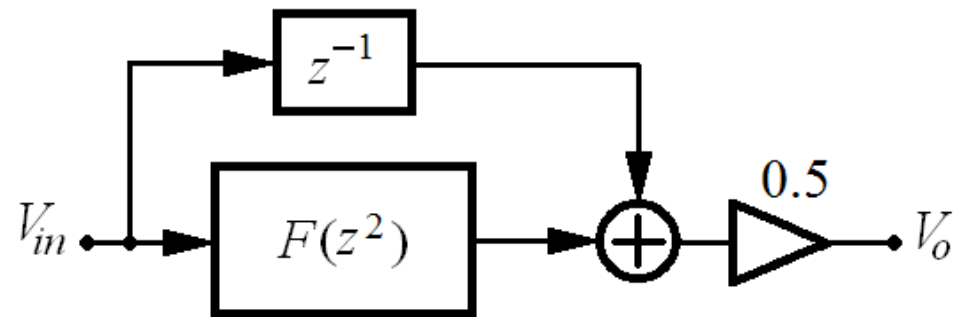
The magnitude frequency response is zero at the angular frequency

$$\omega_n = \cos^{-1} \left(\frac{a - 1}{2a} \right)$$



Capacitance Ratio Measurement Technique

Realization of $H(z)$:

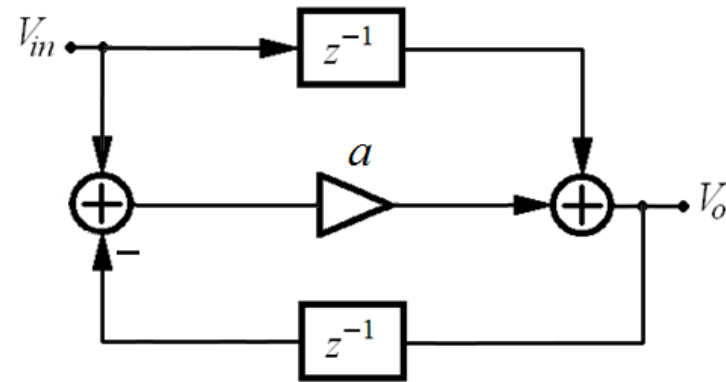


$F(z)$ is the 1st order allpass filter

$$F(z) = \frac{z^{-1} + a}{1 + az^{-1}}$$

Capacitance Ratio Measurement Technique

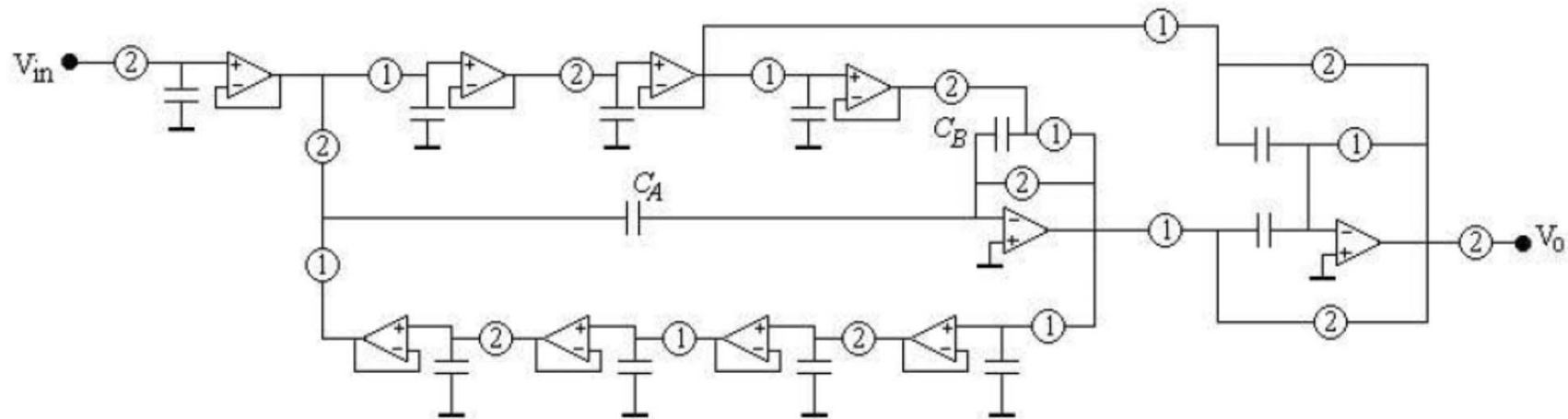
Realization of $F(z)$ by a *structurally* allpass filter:



$$F(z) = \frac{z^{-1} + a}{1 + az^{-1}}$$

Capacitance Ratio Measurement Technique

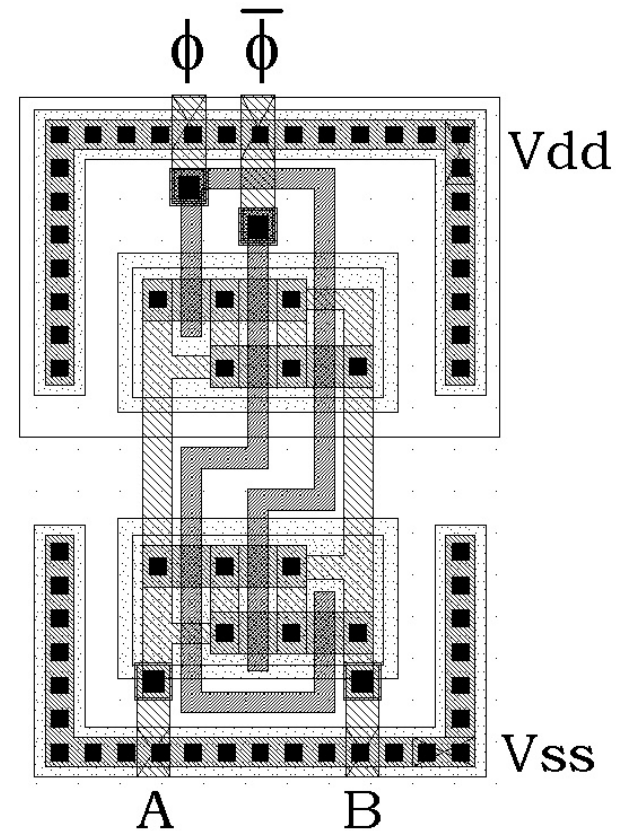
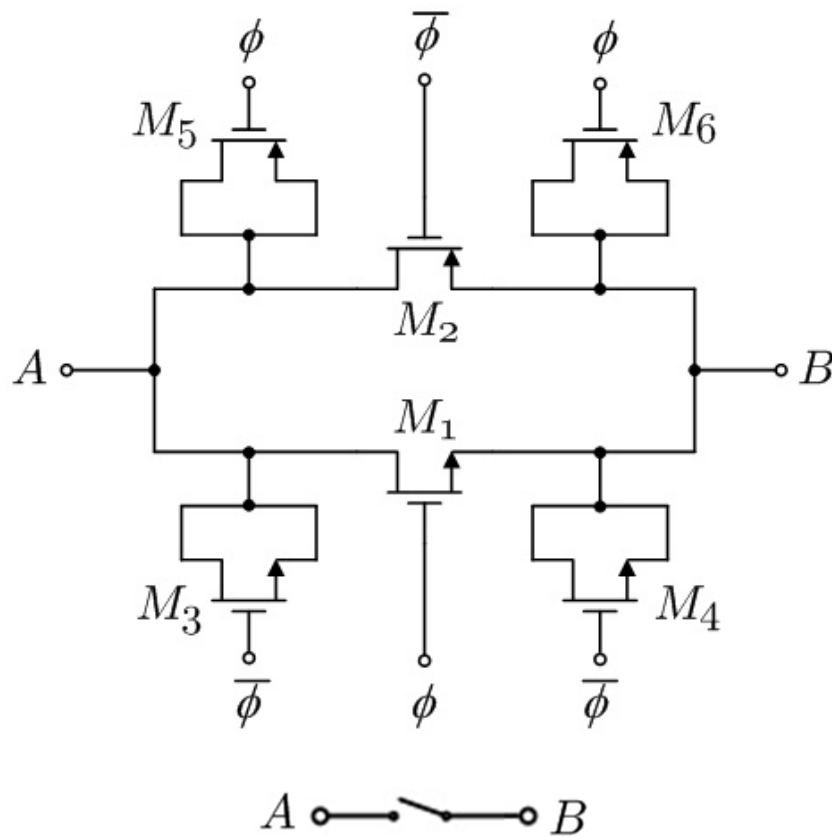
Realization of $F(z^2)$ and the adder:



$$H(z) = \frac{1}{2} \left(\frac{a + z^{-2}}{1 + az^{-2}} + z^{-1} \right)$$

Analog Switches

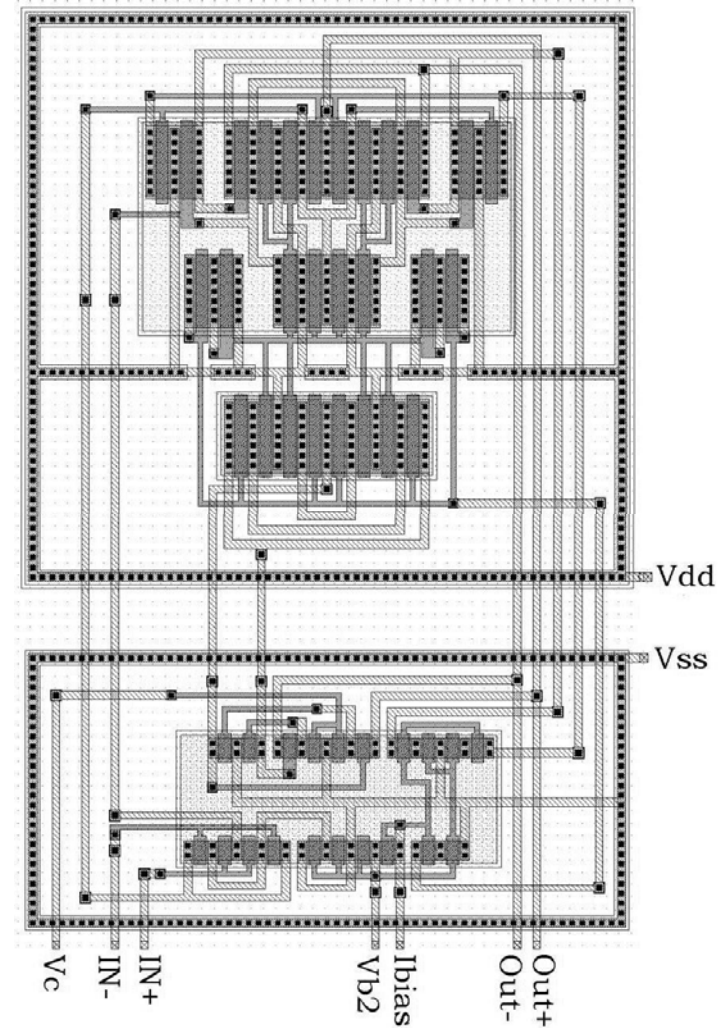
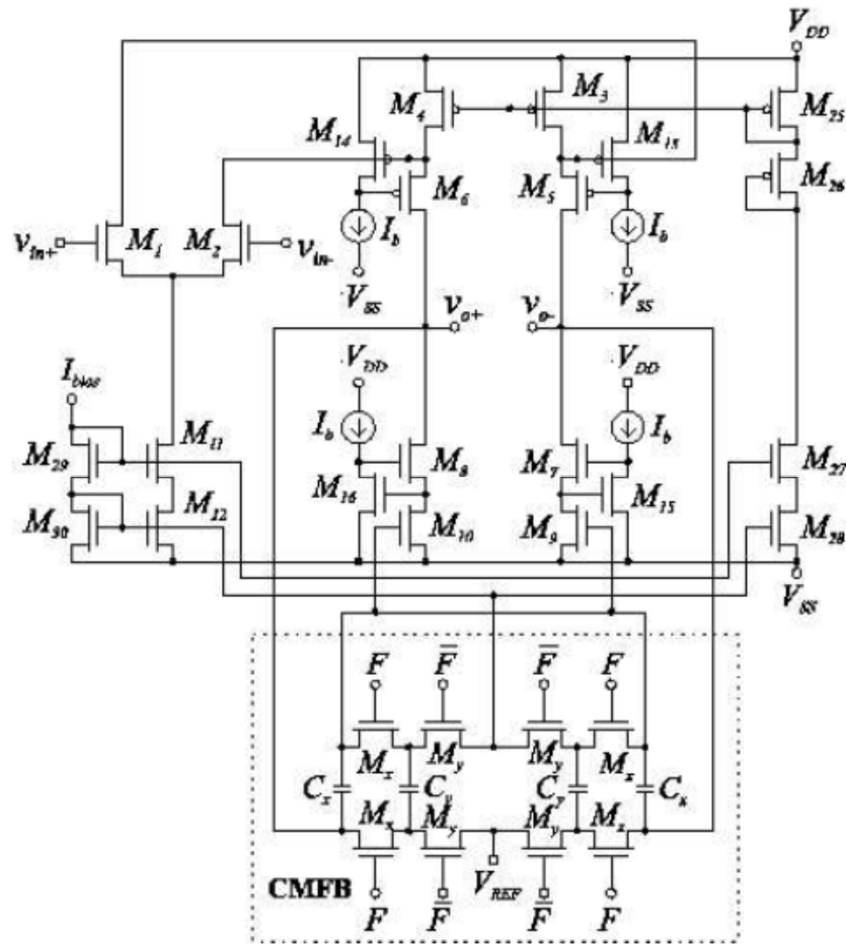
Both complementary and dummy devices were employed to reduce charge injection and clock leakage:



11,5 μm x 15,2 μm
in 0.35 μm CMOS

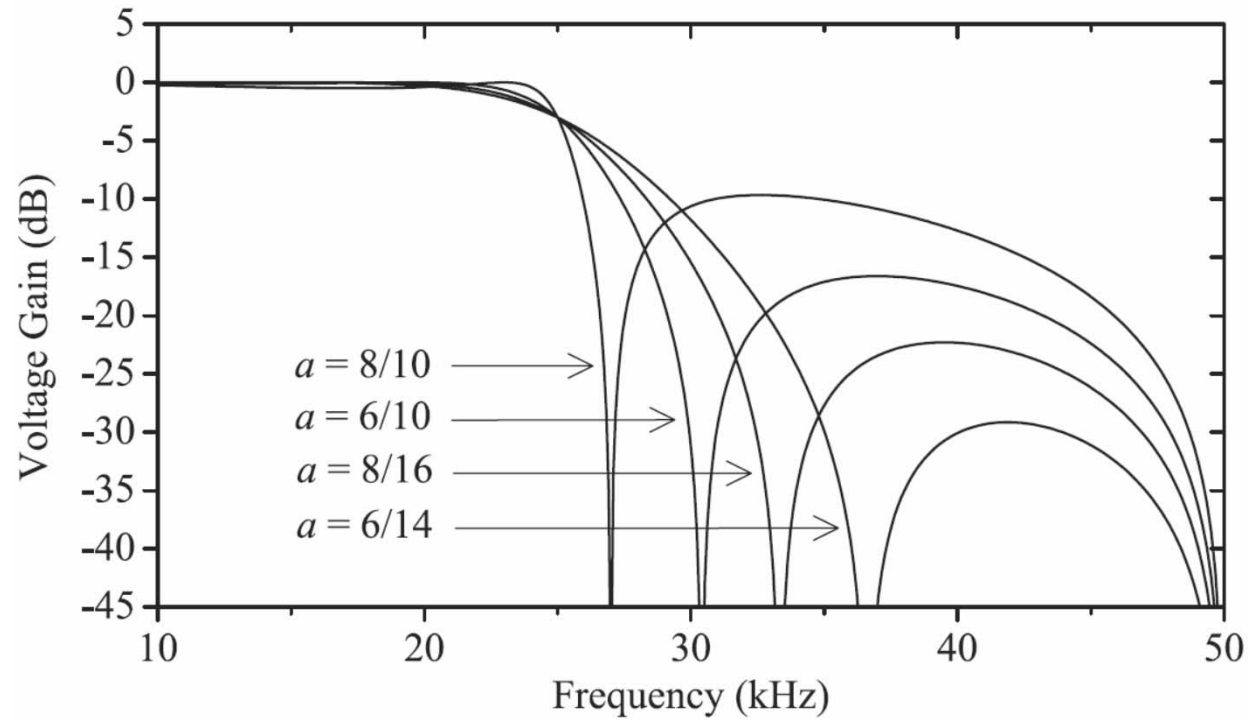
Amplifiers

Fully differential folded cascode amplifier with gain boosting (90 dB)



49,9 μm x 76,2 μm (0.35 μm CMOS)

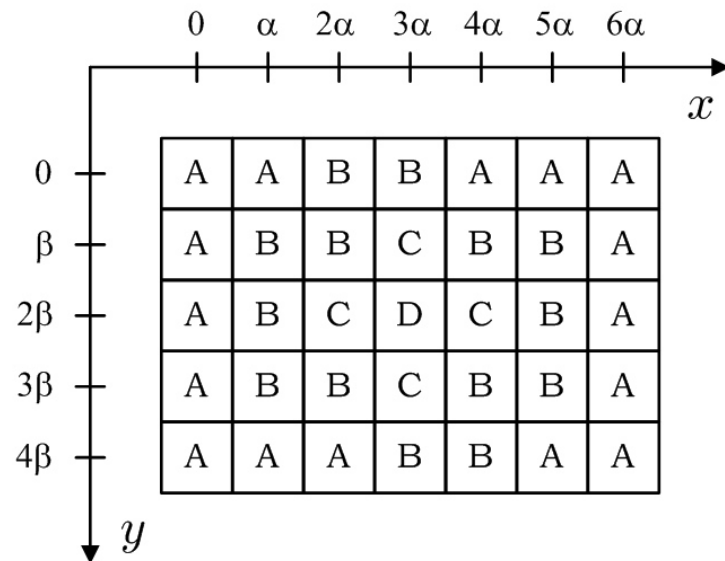
Experimental Results



Frequency responses for 4 different values of $a = C_A/C_B$, and $f_s = 100$ kHz.

Mismatch Caused by Process Gradients

Symmetrical layout with common centroid: evaluation of the mean capacitance of each capacitor, assuming a linear model for t_{ox} variation:



$$\langle C_{xy} \rangle_A = \frac{1}{16} \cdot [16 C_u + 48 \alpha + 32 \beta] = C_u + 3 \alpha + 2 \beta$$

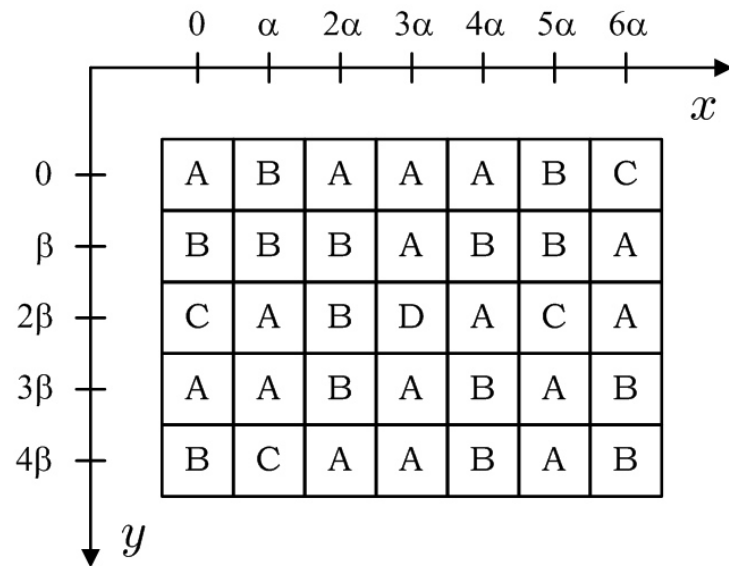
$$\langle C_{xy} \rangle_B = \frac{1}{14} \cdot [14 C_u + 42 \alpha + 28 \beta] = C_u + 3 \alpha + 2 \beta$$

$$\langle C_{xy} \rangle_C = \frac{1}{4} \cdot [4 C_u + 12 \alpha + 8 \beta] = C_u + 3 \alpha + 2 \beta$$

$$\langle C_{xy} \rangle_D = C_u + 3 \alpha + 2 \beta$$

Mismatch Caused by Process Gradients

Asymmetrical layout with common centroid:



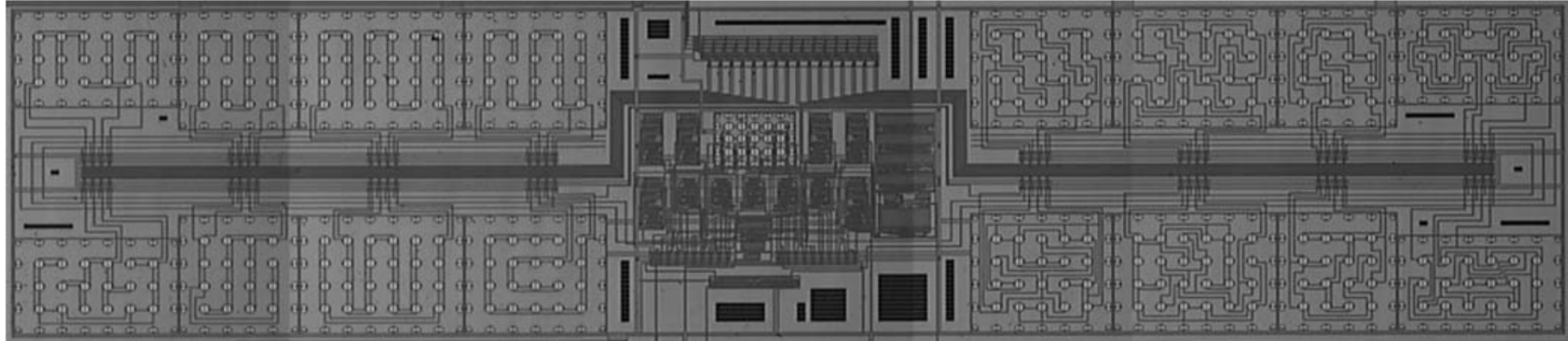
$$\langle C_{xy} \rangle_A = \frac{1}{16} \cdot [16 C_u + 48 \alpha + 32 \beta] = C_u + 3 \alpha + 2 \beta$$

$$\langle C_{xy} \rangle_B = \frac{1}{14} \cdot [14 C_u + 42 \alpha + 28 \beta] = C_u + 3 \alpha + 2 \beta$$

$$\langle C_{xy} \rangle_C = \frac{1}{4} \cdot [4 C_u + 12 \alpha + 8 \beta] = C_u + 3 \alpha + 2 \beta$$

$$\langle C_{xy} \rangle_D = C_u + 3 \alpha + 2 \beta$$

Experimental Results



Process technology: 0.35 μm CMOS

Dimensions: 3.2 x 0.90 mm²

Unit capacitance: 100 fF

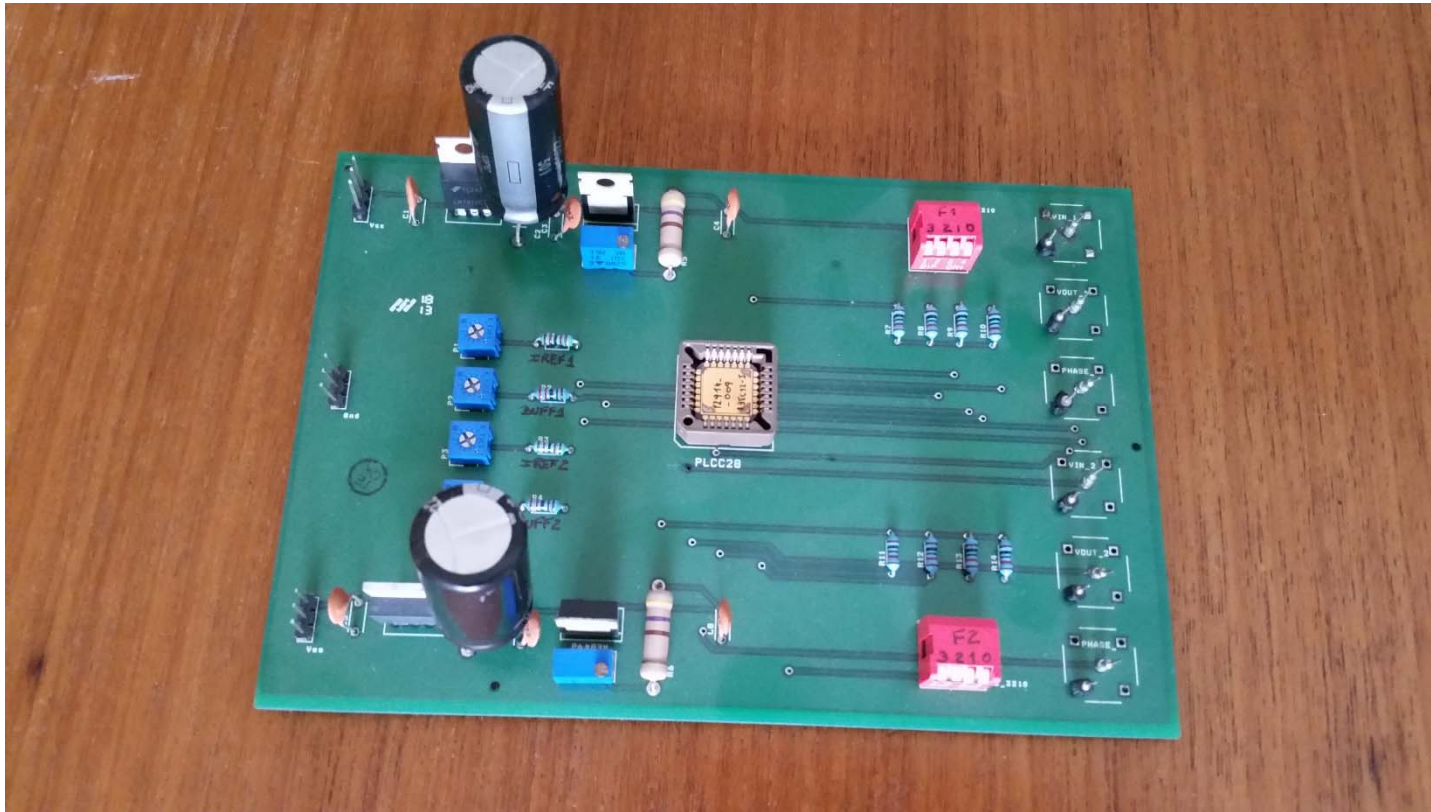
Power supply: ± 2.5 V

Power consumption: 3.13 mW

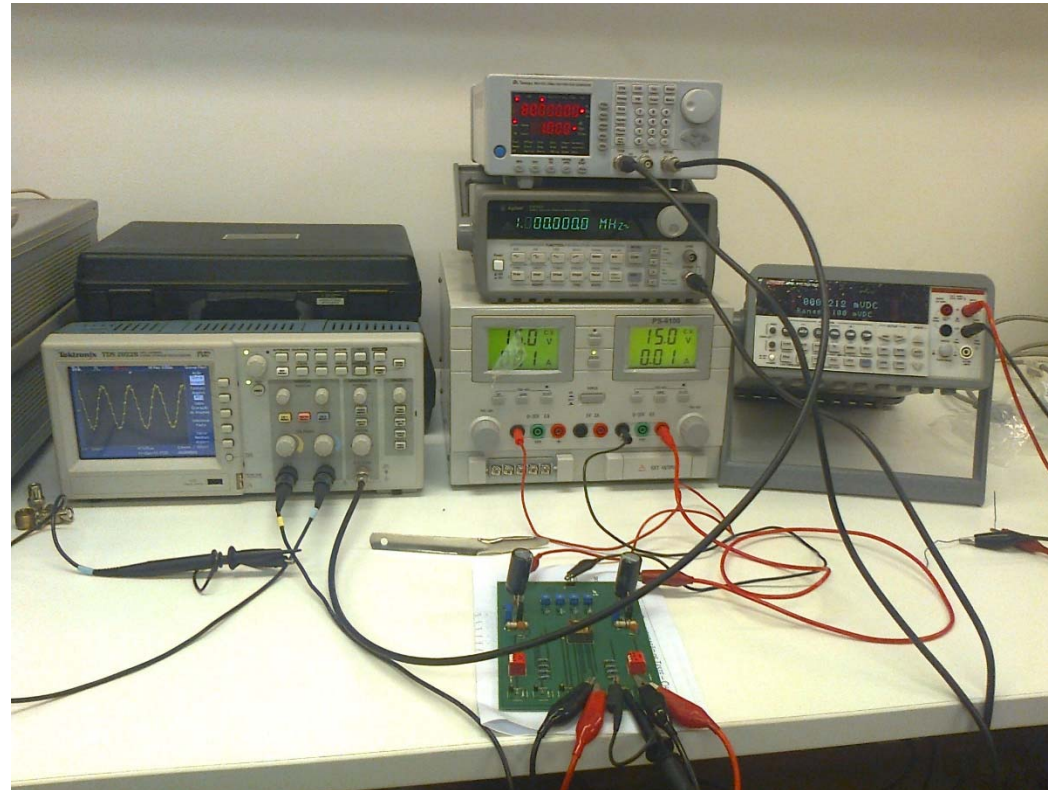
- Frequency responses of 4 capacitance ratio values $C_A/C_B = 6/14, 8/16, 6/10, 8/10$;
- 15 fabricated filters were measured;
- Each capacitance ratio was implemented in 4 different layouts;
- Total of 240 frequency response measurements.

(*) C. F. T. Soares, A. Petraglia and G.S. Campos, "Methodologies for evaluating and measuring capacitance mismatch in CMOS integrated circuits," *IEEE Trans. Circ. Syst. II*, Feb. 2017.

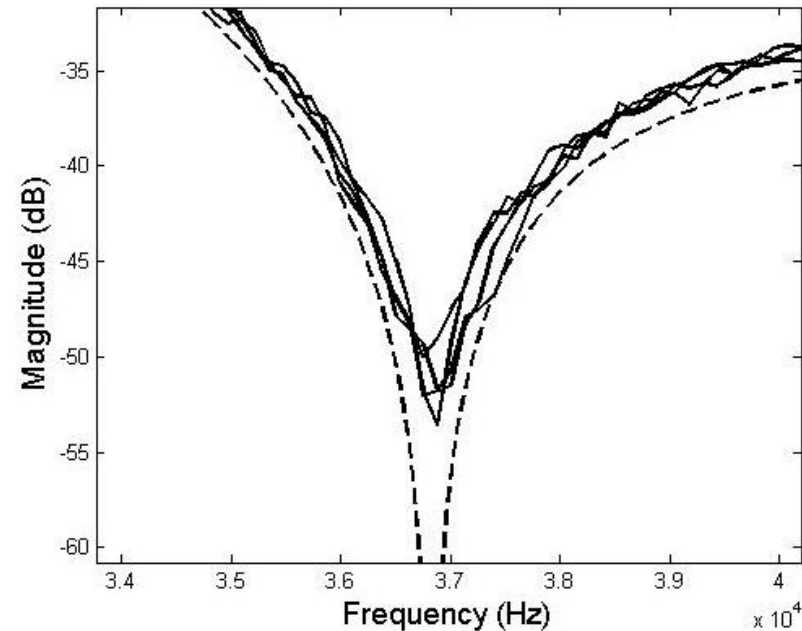
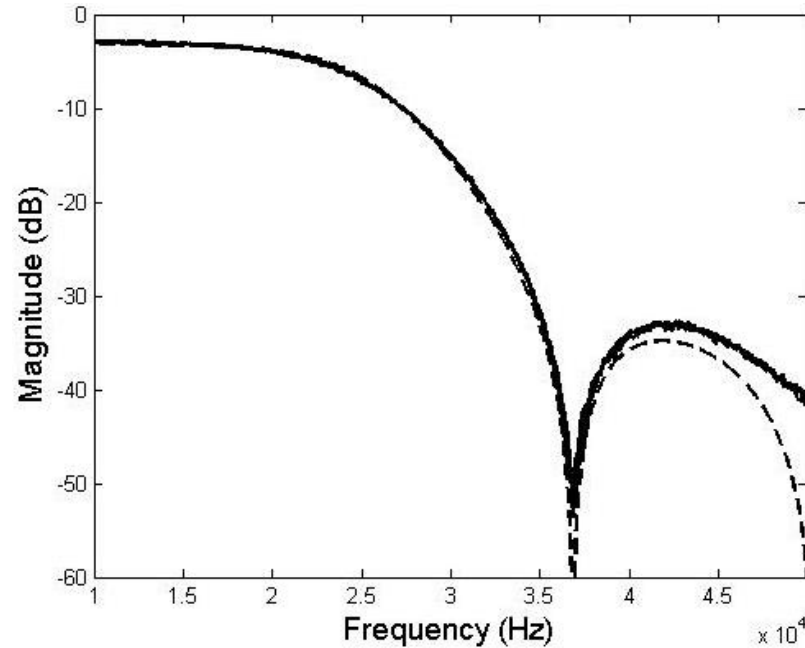
Experimental Results



Experimental Results



Experimental Results



$C_A = 600$ fF; $C_B = 1.4$ pF

Nominal sampling frequency (f_s): 100 kHz

Measured sampling frequency = 100.576 kHz

Theoretical zero frequency = 36.834 kHz

Measured zero frequencies = 36.752 kHz and 36.880 kHz

Ideal capacitance ratio = $6/14 = 0.429$

Measured capacitance ratios = 0.4279, 0.4281, 0.4292, 0.4294

Mean error = - 0.082%

Experimental Results

A	A	B	B	B
A	A	B	B	B
A	B	B	B	B
A	B	B	B	B

(a)

B	B	B	B	B
B	A	A	A	B
B	A	A	A	B
B	B	B	B	B

(b)

B	A	B	B	A
B	B	A	B	B
A	B	B	B	A
B	B	A	B	B

(c)

B	B	A	B	B
A	B	B	A	B
B	A	B	B	A
B	B	A	B	B

(d)

Capacitance matrices to implement $C_A/C_B = 3/7$ using $N_A = 6$ and $N_B = 14$ in different arrangements:

- (a) without layout technique to improve matching;
- (b) symmetric arrangement in common centroid, without correlation coefficient maximization between C_A and C_B ;
- (c) without common centroid, but correlation between C_A and C_B optimized;
- (d) common centroid arrangement and correlation between C_A and C_B optimized.

Experimental Results

A	A	B	B	B	B
A	A	B	B	B	B
A	A	B	B	B	B
A	A	B	B	B	B

(a)

A	B	B	B	B	A
A	B	B	B	B	A
A	B	B	B	B	A
A	B	B	B	B	A

(b)

B	A	B	B	A	B
A	B	B	A	B	B
B	B	A	B	A	B
A	B	B	A	B	B

(c)

B	A	B	B	A	B
B	B	A	B	B	A
A	B	B	A	B	B
B	A	B	B	A	B

(d)

Capacitance matrices to implement $C_A/C_B = 1/2$ using $N_A = 8$ and $N_B = 16$ in different arrangements:

- (a) without layout technique to improve matching;
- (b) symmetric arrangement in common centroid, without correlation coefficient maximization between C_A and C_B ;
- (c) without common centroid, but correlation between C_A and C_B optimized;
- (d) common centroid arrangement and correlation between C_A and C_B optimized.

Experimental Results

A	A	B	B
A	A	B	B
A	B	B	B
A	B	B	B

(a)

A	B	B	B
A	B	B	A
A	B	B	A
B	B	B	A

(b)

A	B	B	A
B	A	B	B
A	B	A	A
B	B	B	B

(c)

A	B	B	A
B	A	B	B
B	B	A	B
A	B	B	A

(d)

Capacitance matrices to implement $C_A/C_B = 3/5$ using $N_A = 6$ and $N_B = 10$ in different arrangements:

- (a) without layout technique to improve matching;
- (b) symmetric arrangement in common centroid, without correlation coefficient maximization between C_A and C_B ;
- (c) without common centroid, but correlation between C_A and C_B optimized;
- (d) common centroid arrangement and correlation between C_A and C_B optimized.

Experimental Results

A	A	A	B	B	B
A	A	A	B	B	B
A	A	B	B	B	B

(a)

B	B	A	A	B	B
B	A	A	A	A	B
B	B	A	A	B	B

(b)

B	A	B	A	B	A
B	A	B	B	A	B
B	A	B	A	B	A

(c)

B	A	B	B	A	B
A	B	A	A	B	A
B	A	B	B	A	B

(d)

Capacitance matrices to implement $C_A/C_B = 4/5$ using $N_A = 8$ and $N_B = 10$ in different arrangements:

- (a) without layout technique to improve matching;
- (b) symmetric arrangement in common centroid, without correlation coefficient maximization between C_A and C_B ;
- (c) without common centroid, but correlation between C_A and C_B optimized;
- (d) common centroid arrangement and correlation between C_A and C_B optimized.

Experimental Results

Averages and variances of measured transmission zero frequencies, showing common centroid errors and correlation coefficients of capacitance ratios C_A/C_B

C_A/C_B	IDEAL ZERO FREQ. (kHz)	LAYOUT IN FIG.	CENTROID ERROR	CORRELATION COEF.	AVERAGE MEAS. ZERO FREQ. (kHz)	VARIANCE
6/14	36.614	6(a)	0.2736	0.8754	36.244	0.0263
		6(b)	0.0000	0.9700	36.357	0.0124
		6(c)	0.0053	0.9886	36.446	0.0086
		6(d)	0.0000	0.9896	36.598	0.0032
8/16	33.333	7(a)	0.2941	0.8419	33.218	0.0207
		7(b)	0.0000	0.9558	33.233	0.0231
		7(c)	0.0103	0.9877	33.303	0.0039
		7(d)	0.0000	0.9923	33.294	0.0024
6/10	30.409	8(a)	0.2225	0.9017	30.384	0.0062
		8(b)	0.0000	0.9726	30.414	0.0052
		8(c)	0.0168	0.9832	30.429	0.0067
		8(d)	0.0000	0.9879	30.405	0.0016
8/10	26.995	9(a)	0.3004	0.8394	26.984	0.0037
		9(b)	0.0000	0.9605	26.983	0.0027
		9(c)	0.0159	0.9855	26.979	0.0025
		9(d)	0.0000	0.9919	26.958	0.0024

