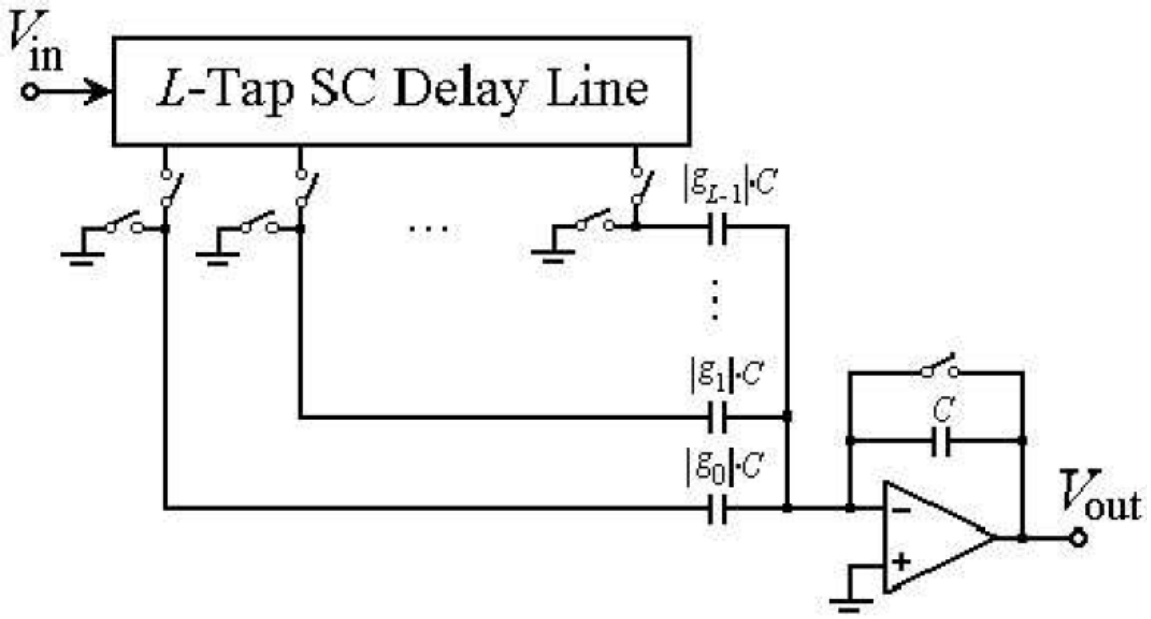
Direct-Form SC Filters

Direct-Form FIR SC Filter Realization

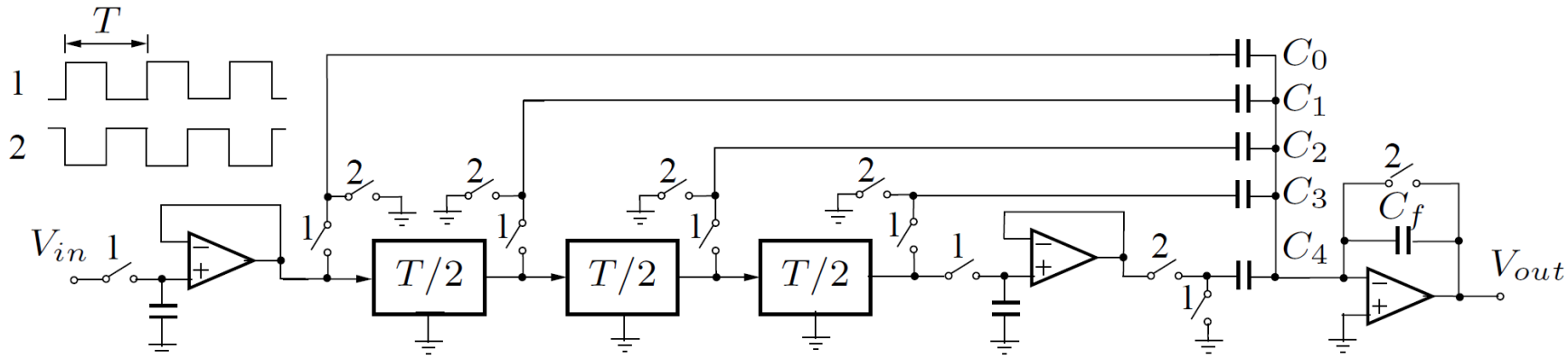
(L-1)th-order FIR SC filter:

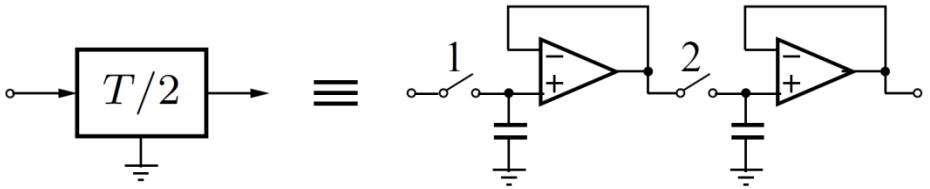


$$\frac{V_{out}}{V_{in}}(z) = \sum_{k=0}^{L-1} g_k z^{-k}$$

Direct-Form FIR SC Filter Realization

Ex.: 4th-order SC FIR filter

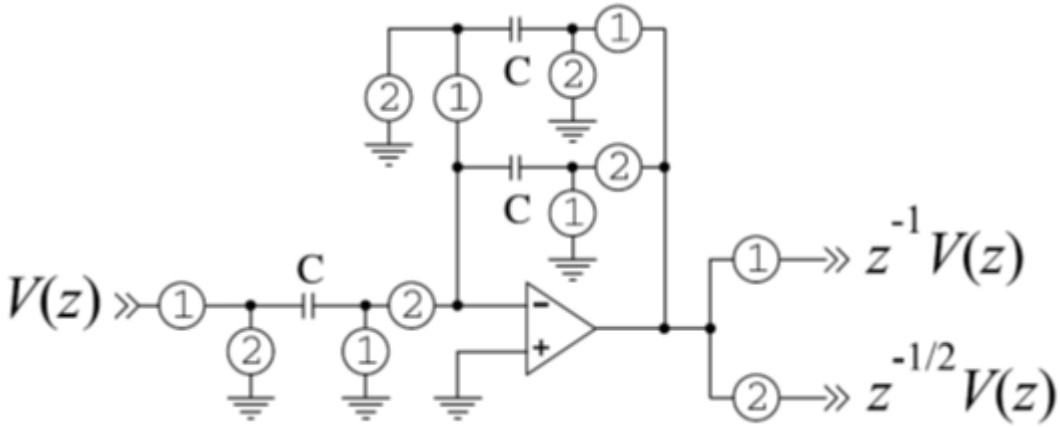




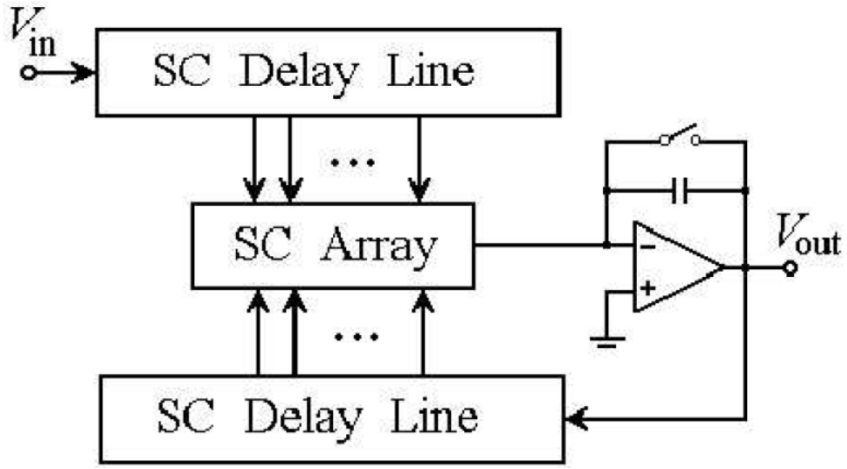
$$\frac{V_{out}}{V_{in}}(z) = -\frac{C_0}{C_f} - \frac{C_1}{C_f}z^{-1} - \frac{C_2}{C_f}z^{-2} - \frac{C_3}{C_f}z^{-3} + \frac{C_4}{C_f}z^{-4}$$

Direct-Form FIR SC Filter Realization

Reduction of the number of amplifiers by a multiplexing technique



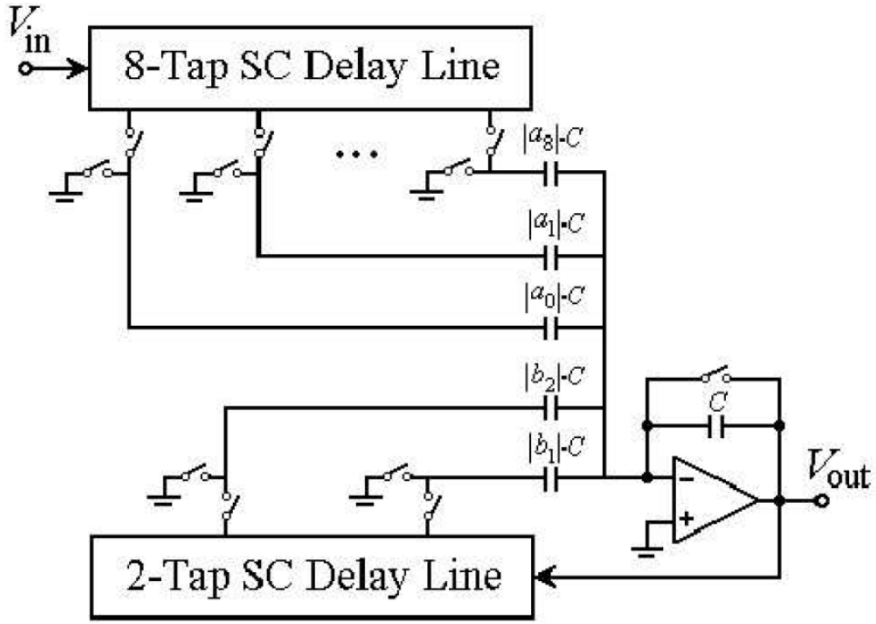
Direct-Form IIR SC Filter Realization



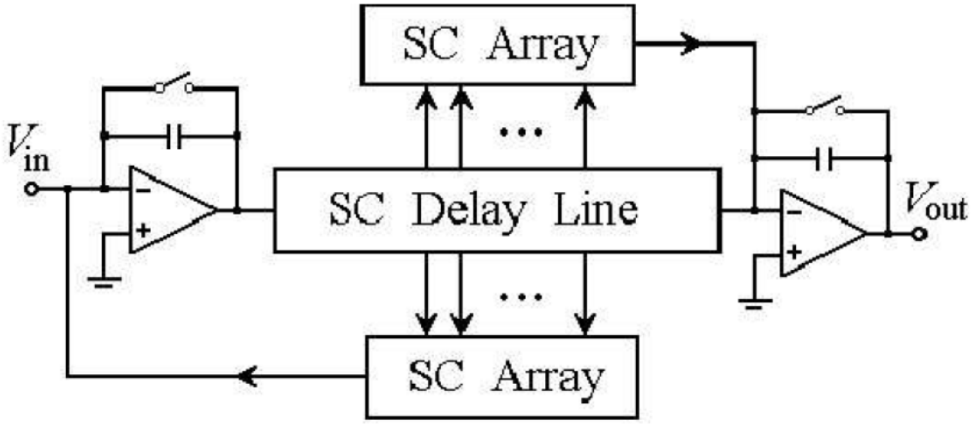
Direct Form I

2 SC delay lines sharing the same SC array

Ex.: $\frac{V_{out}}{V_{in}}(z) = \frac{a_0 + a_1 z^{-1} + \cdots + a_8 z^{-8}}{1 - b_1 z^{-1} - b_2 z^{-2}}$



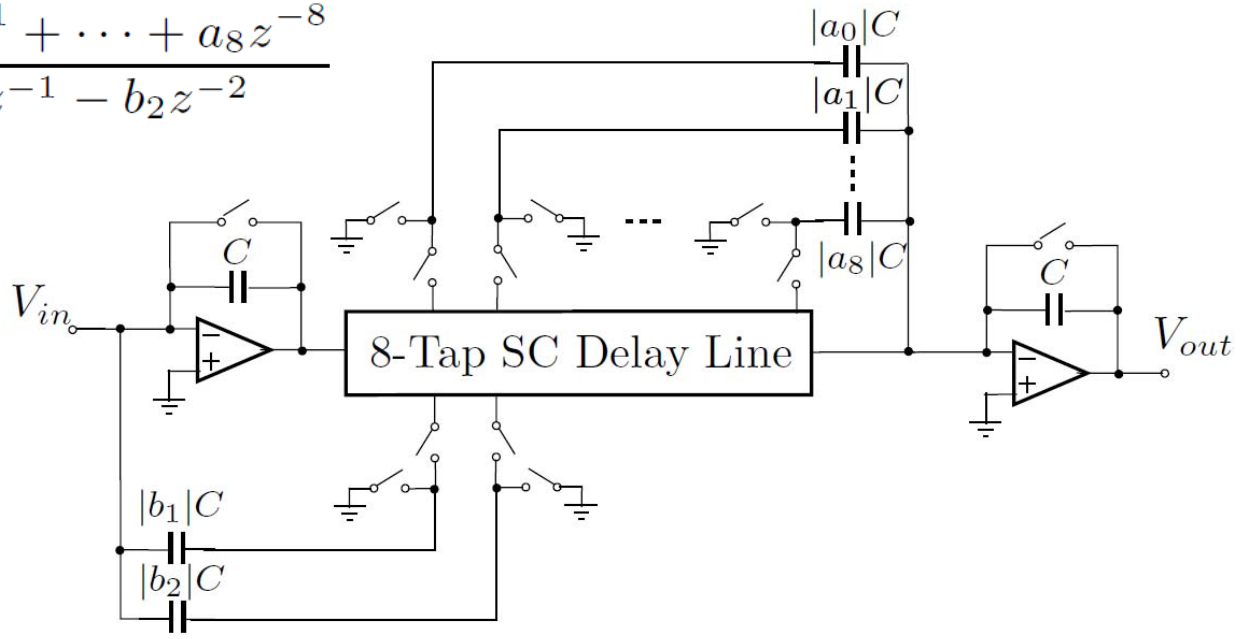
Direct-Form IIR SC Filter Realization



Direct Form II

2 SC arrays sharing the same SC delay line

Ex.: $\frac{V_{out}}{V_{in}}(z) = \frac{a_0 + a_1 z^{-1} + \cdots + a_8 z^{-8}}{1 - b_1 z^{-1} - b_2 z^{-2}}$



Capacitors in CMOS Technology

Aplications in which capacitance matching is critical issue:

- Converters: A/D, D/A, DC/DC
- Switched-capacitor filters

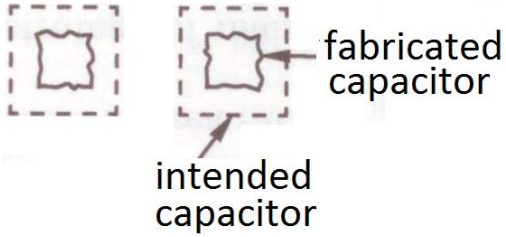
Capacitance mismatch sources in CMOS IC's:

- Process gradient (t_{ox})
- Random errors

Capacitors in CMOS Technology

Capacitors too small:

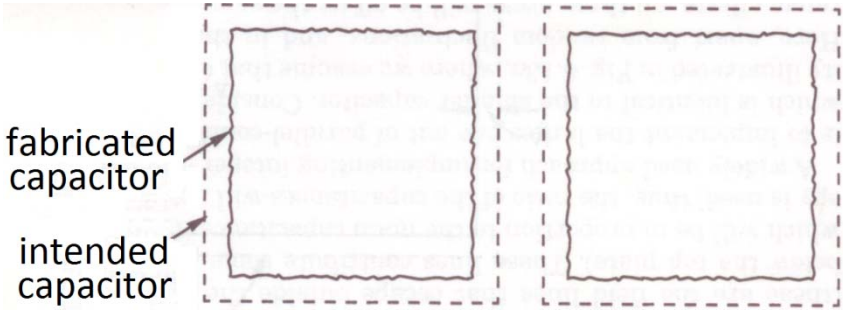
– The actual capacitance ratio can be significantly different from unity.



Larger capacitors:

– Better ratio accuracy;

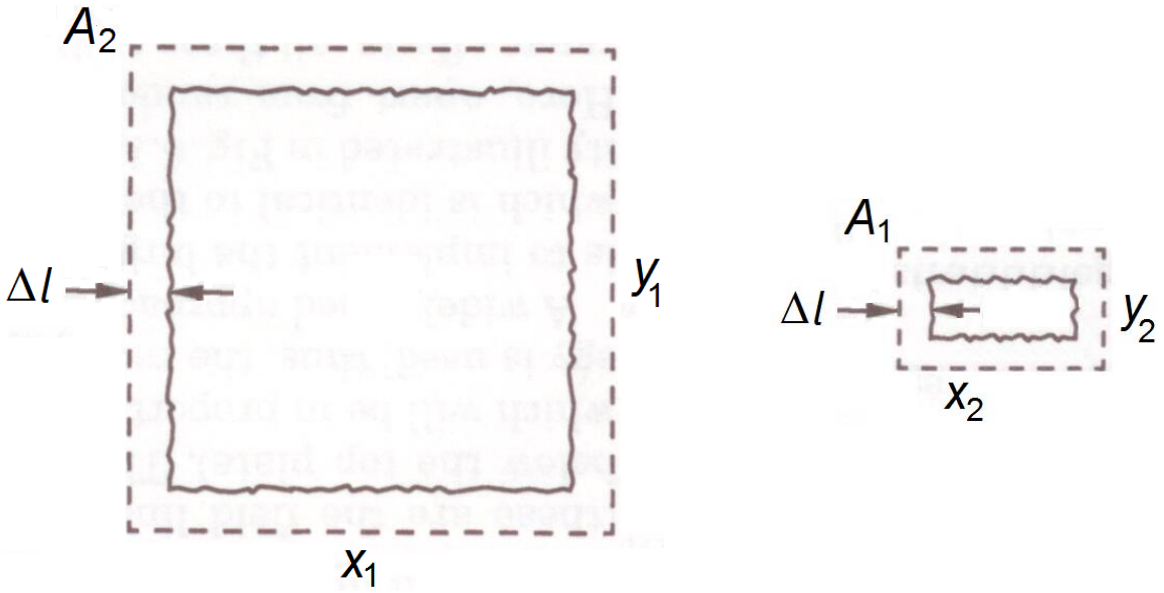
– However, if the plates are too large: (i) chip area may be excessive;
(ii) opposite regions of the two capacitors may be affected differently by the fabrication process (e.g., slightly difference in oxide thickness);



Capacitors in CMOS Technology

Sistematic errors:

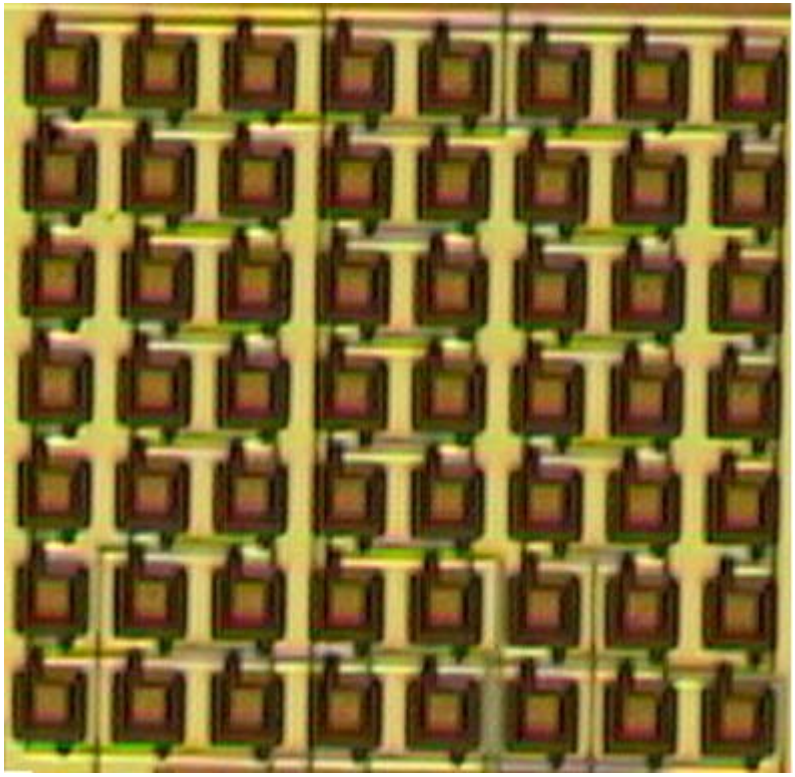
- The relative area error of two capacitors will be the same if the nominal perimeter/area ratio is the same;
- Therefore the capacitance ratio will not be affected.



Capacitor Layout

Techniques to improve capacitance matching:

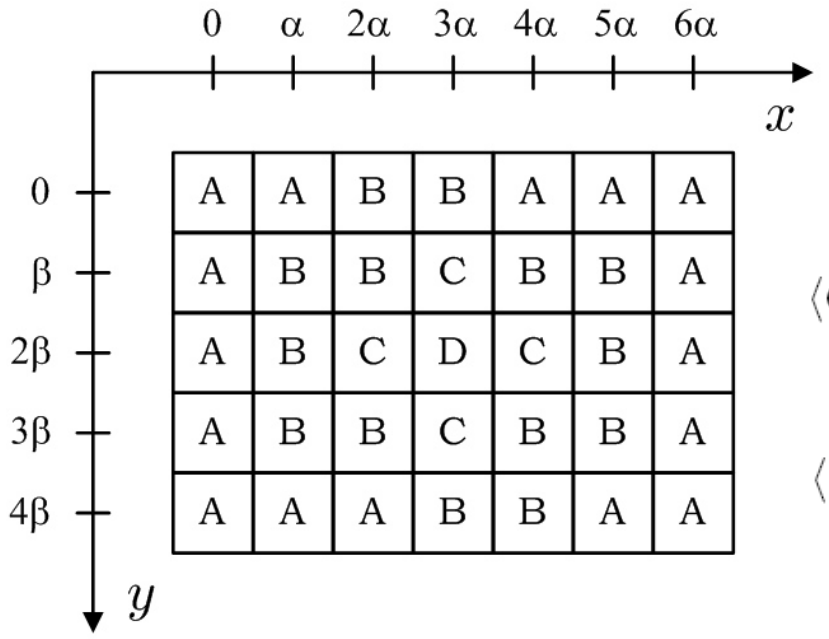
- Parallel connection of identical unit capacitors to implement each capacitance;
- Arrangement of unit capacitors in common centroid symmetry;
- Careful routing inside capacitor matrices.



Unit capacitor arrangement:
C = 100 fF, 5µmx5µm

Capacitor Layout

Common centroid geometry - evaluation of the mean unit capacitance of each capacitor, assuming the linear model for t_{ox}:



$$\langle C_{xy} \rangle_A = \frac{1}{16} \cdot [16\,C + 48\,\alpha + 32\,\beta] = C + 3\,\alpha + 2\,\beta$$

$$\langle C_{xy} \rangle_B = \frac{1}{14} \cdot [14\,C + 42\,\alpha + 28\,\beta] = C + 3\,\alpha + 2\,\beta$$

$$\langle C_{xy} \rangle_C = \frac{1}{4} \cdot [4\,C + 12\,\alpha + 8\,\beta] = C + 3\,\alpha + 2\,\beta$$

$$\langle C_{xy} \rangle_D = C + 3\,\alpha + 2\,\beta$$

Capacitor Layout

Difficulties:

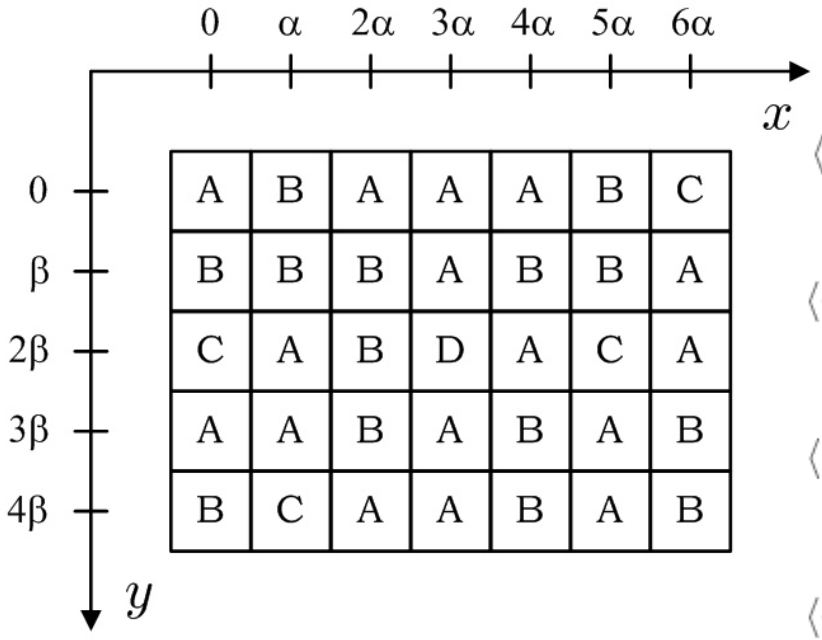
- Common centroid arrangement is not a simple task when the number of capacitance ratios is large;
- Common centroid geometry is not always possible;
- When it is possible, there are several alternatives;

Solutions:

- Develop an algorithm to search for the best arrangement among different possibilities;
- Find the optimal arrangement that doesn't have symmetry when common centroid is not possible.

Capacitor Layout

Example without common centroid, but insensitive to process gradient:



$$\langle C_{xy} \rangle_A = \frac{1}{16} \cdot [16\,C + 48\,\alpha + 32\,\beta] = C + 3\,\alpha + 2\,\beta$$

$$\langle C_{xy} \rangle_B = \frac{1}{14} \cdot [14\,C + 42\,\alpha + 28\,\beta] = C + 3\,\alpha + 2\,\beta$$

$$\langle C_{xy} \rangle_C = \frac{1}{4} \cdot [4\,C + 12\,\alpha + 8\,\beta] = C + 3\,\alpha + 2\,\beta$$

$$\langle C_{xy} \rangle_D = C + 3\,\alpha + 2\,\beta$$

C.F.T. Soares, A.C.M. Filho and A. Petraglia, *IEEE Trans. Evolutionary Computation*, Jun. 2010.

Capacitance Mismatch Effects

Mathematical model commonly used in computer aided analysis of SC filters:

$$\hat{\gamma_k} = \gamma_k + \epsilon_{\gamma_k}$$

were $\epsilon_{\gamma_k} = \gamma_k \epsilon_k$

γ_k : capacitance ratios

ϵ_k : uncorrelated zero-mean Gaussian random variables

Capacitance Mismatch Effects

Ex.: Frequency responses of 3 FIR filters having $L = 50$ and $\sigma_\epsilon = 0.001$