Analog Decimation Filters

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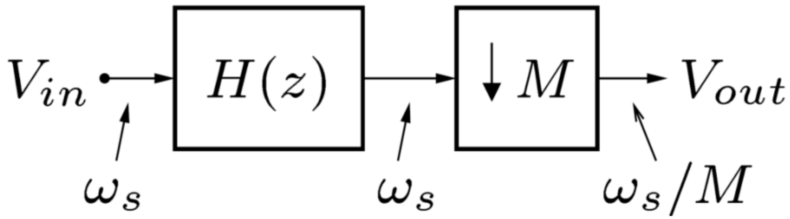
Decimation and Interpolation Filters

Decimation Filter

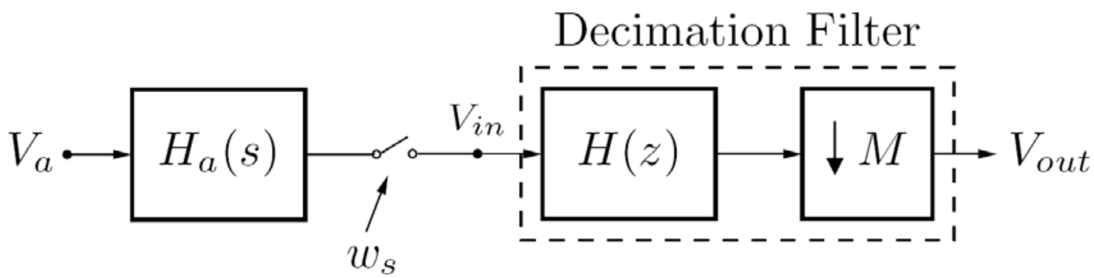


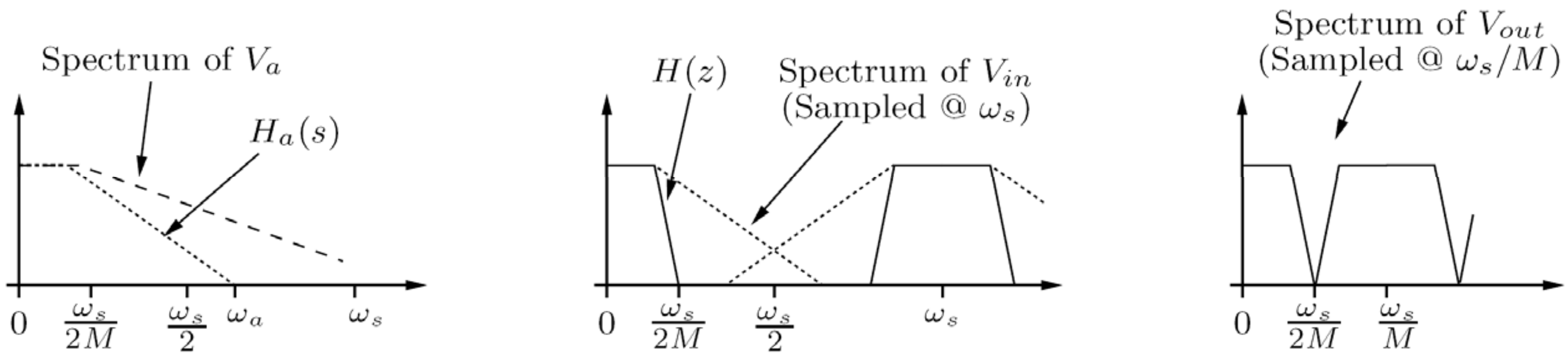
Ideal Frequency Response

$$H(e^{j\omega}) = \begin{cases} 1, & |\omega| \leq \omega_s/2M \\ 0, & \omega_s/2M < |\omega| \leq \omega_s/2 \end{cases}$$

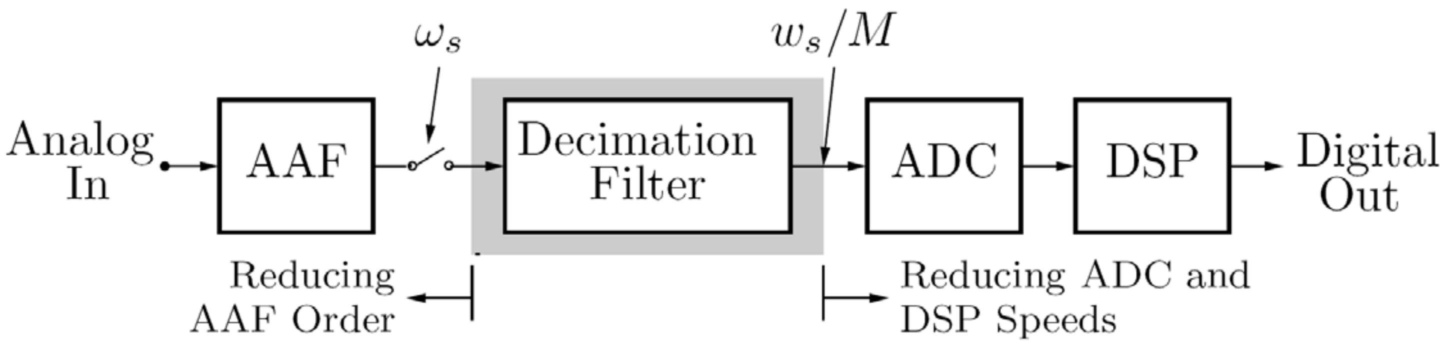
- The cascade of a lowpass filter and a down-sampler is called a *decimation filter*;
- Filter *H*(*z*) attenuates input frequency components greater than $\omega_s/2M$;
- The sampling rate can then be reduced by the factor *M*.

Sampling of Analog Signals





Sampling of Analog Signals



- Output of the anti-aliasing filter (AAF) is oversampled by factor *M*:
  → transition band of AAF can be increased;
- Accurate bandlimiting provided by SC filter H(z) allows sampling rate reduction:
  → reduction of ADC and DSP power consumption.

Efficient Decimation Filter Design

FIR Decimation Filters

$$H(z) = h(0) + h(1)z^{-1} + h(2)z^{-2} + ... + h(7)z^{-7}$$

$$= \underbrace{h(0) + h(3)z^{-3} + h(6)z^{-6}}_{H_0(z^3)} + z^{-1}\underbrace{\left(h(1) + h(4)z^{-3} + h(7)z^{-6}\right)}_{H_1(z^3)} + z^{-2}\underbrace{\left(h(2) + h(5)z^{-3}\right)}_{H_2(z^3)}$$

$$= H_0(z^3) + z^{-1}H_1(z^3) + z^{-2}H_2(z^3)$$

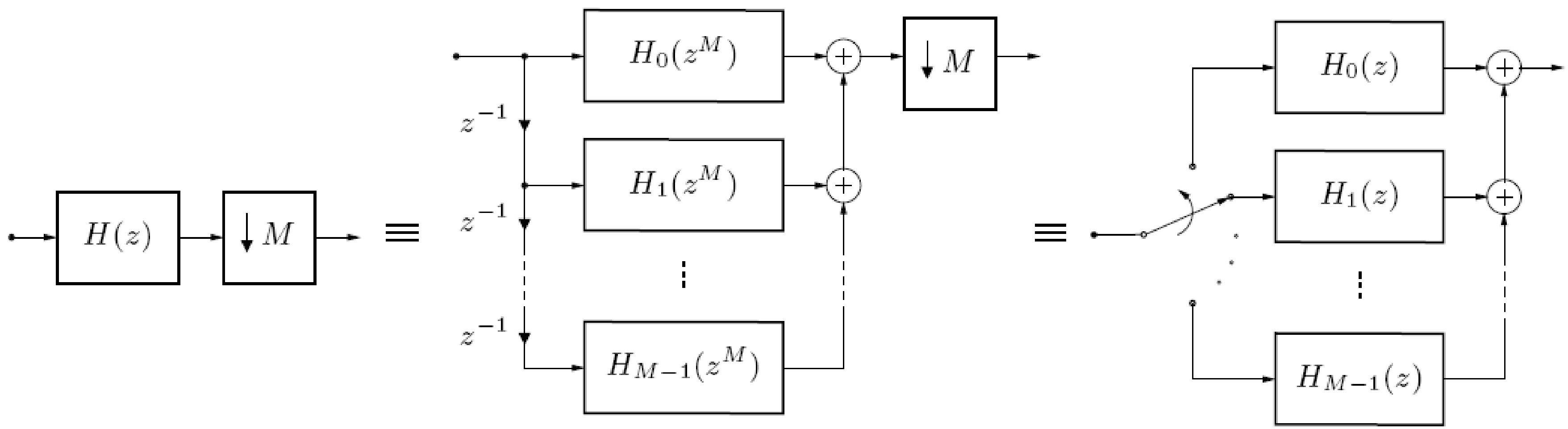
In the general case:

$$H(z) = \sum_{n=0}^{N-1} h(n)z^{-n} = \sum_{k=0}^{M-1} z^{-k}H_k(z^M)$$

Efficient Decimation Filter Design

FIR Decimation Filters

$$H(z) = \sum_{n=0}^{N-1} h(n) z^{-n} = \sum_{k=0}^{M-1} z^{-k} H_k(z^M)$$

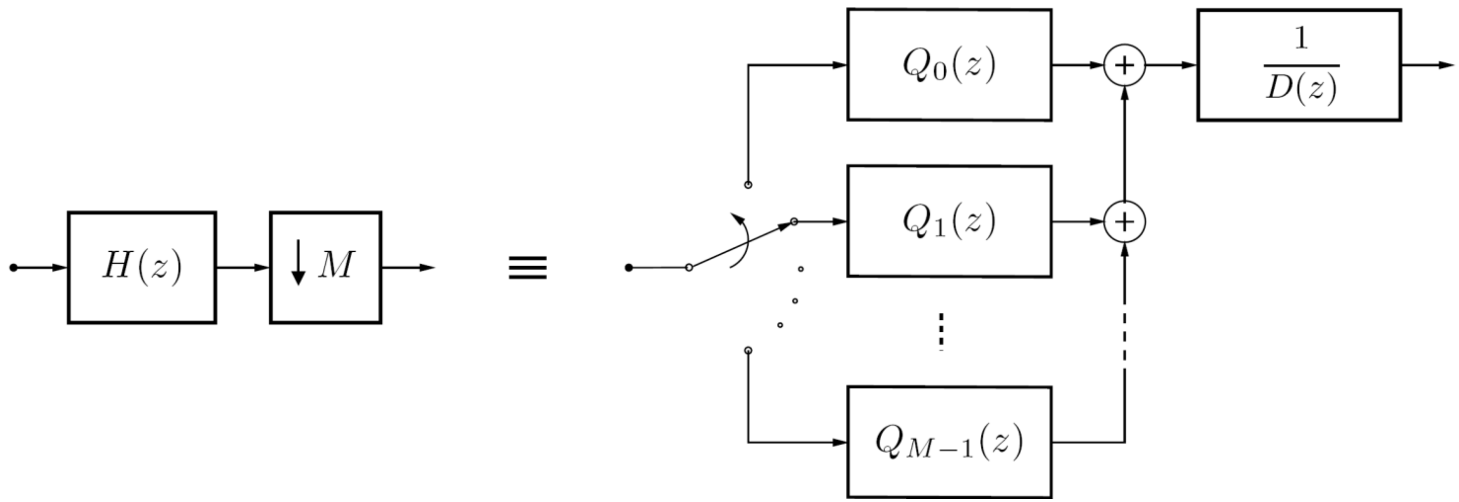


Efficient Decimation Filter Design

IIR Decimation Filters

$$H(z) = \frac{A(z)}{B(z)} = \frac{A(z)P(z)}{B(z)P(z)} = \frac{Q(z)}{D(z^M)} = \frac{\sum_{k=0}^{M-1} z^{-k} Q_k(z^M)}{D(z^M)}$$

$$H(z) = \sum_{k=0}^{M-1} z^{-k} H_k(z^M) \qquad H_k(z) = \frac{Q_k(z)}{D(z)}$$



Efficient Decimation Filter Design

Design Example

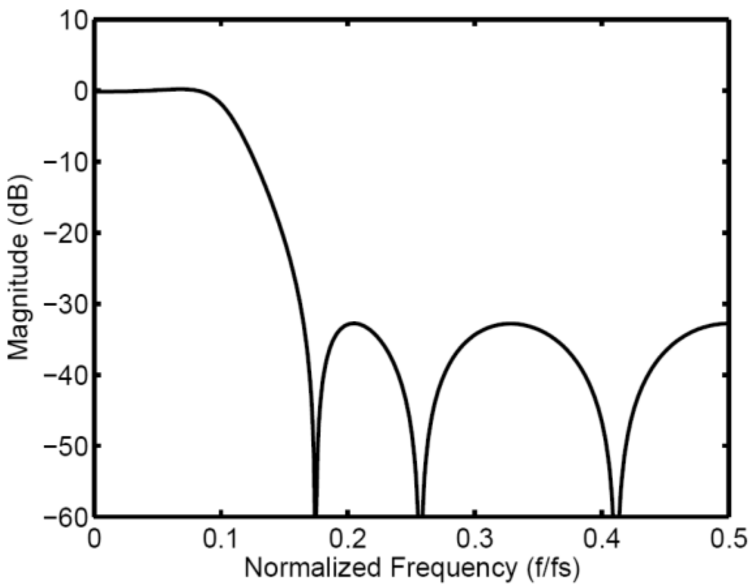
- passband edge frequency = 2.5 MHz
- stopband edge frequency = 4.5 MHz
- passband ripple < 0.4 dB
- stopband attenuation > 25 dB
- Decimation factor $M = 3$
- Input sampling rate = 30 MHz

Efficient Decimation Filter Design

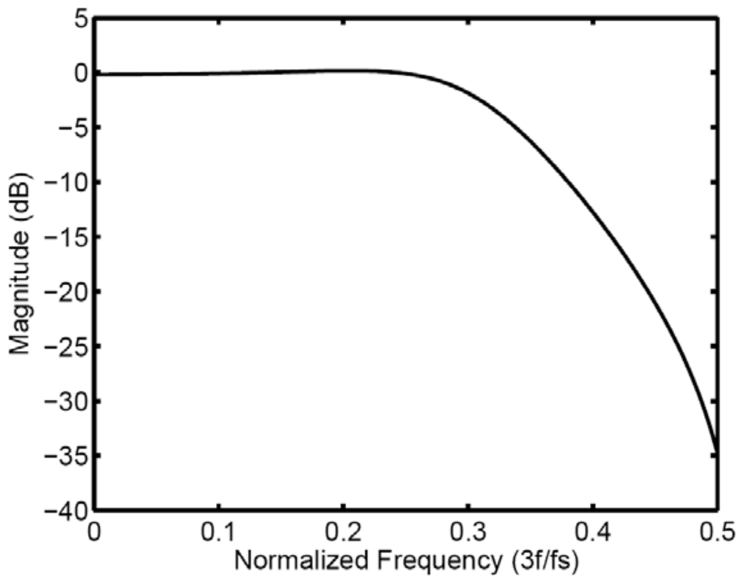
The filter transfer function has been designed with 6 zeros and 2 poles

- low sensitivity to coefficient errors -> small capacitance spread
- small circuit complexity -> low power consumption

Before down-sampling



After down-sampling



Efficient Decimation Filter Design

The filter transfer function has been designed with 6 zeros and 2 poles

$$
\begin{aligned}
a_0 &= 0.0405 \\
a_1 &= 0.0353 \\
a_2 &= 0.0615 \\
a_3 &= 0.0651 \\
a_4 &= 0.0615 \\
a_5 &= 0.0353 \\
a_6 &= 0.0405
\end{aligned}
$$

$$
\begin{aligned}
b_0 &= 1.0000 \\
b_1 &= -1.3166 \\
b_2 &= 0.6631
\end{aligned}
$$

$$H(z) = \frac{A(z)}{B(z)} = \frac{A(z)P(z)}{B(z)P(z)} = \frac{Q(z)}{D(z^M)} = \frac{\sum_{k=0}^{M-1} z^{-k} Q_k(z^M)}{D(z^M)}$$

$$P(z) = 1 + 1.317z^{-1} + 1.070z^{-2} + 0.873z^{-3} + 0.4397z^{-4}$$

$$B(z)P(z) = 1 + 0.3369z^{-3} + 0.215z^{-6}$$

$$D(z) = 1 + 0.3369z^{-1} + 0.215z^{-2}$$

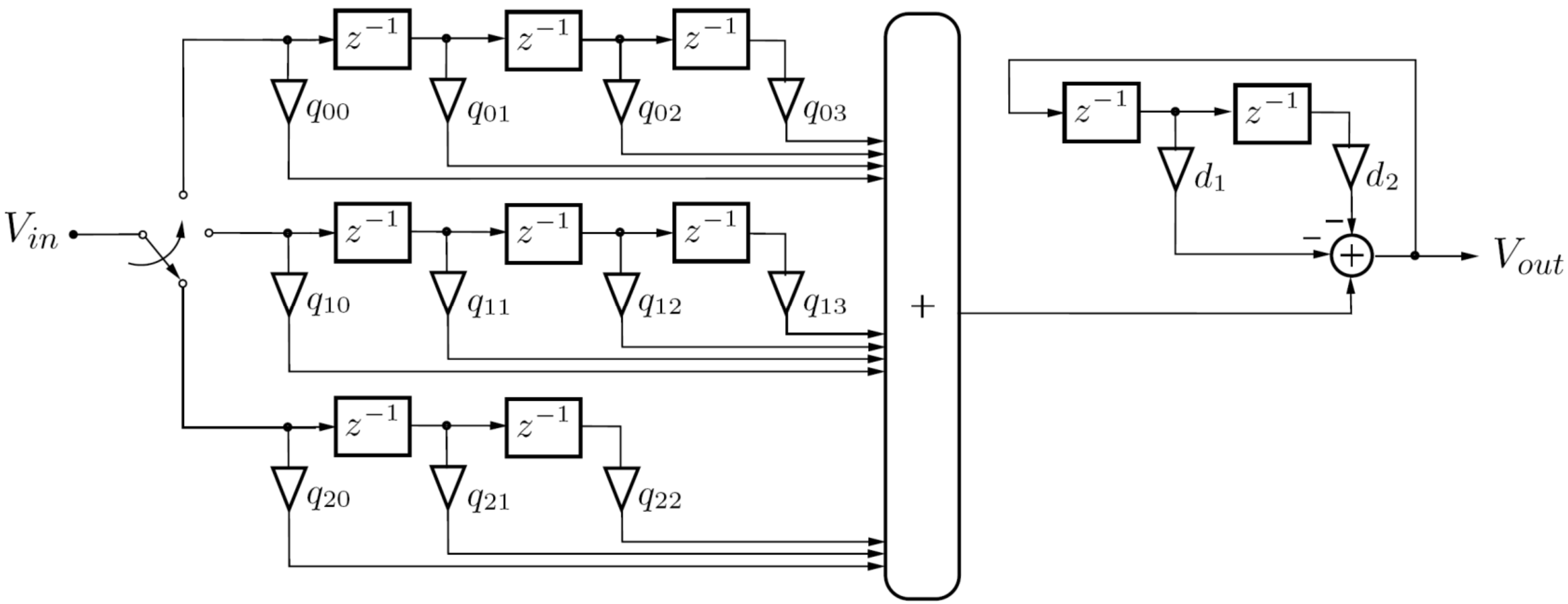
Efficient Decimation Filter Design

Coefficients of the polyphase components

$H(z)$	$Q_k(z)$	$D(z)$
$a_0 = 0.0405$	$q_{00} = 0.0405$	$d_0 = 1.0000$
$a_1 = 0.0353$	$q_{01} = 0.2192$	$d_1 = 0.3369$
$a_2 = 0.0615$	$q_{02} = 0.2366$	$d_2 = 0.2915$
$a_3 = 0.0651$	$q_{03} = 0.0509$	
$a_4 = 0.0615$	$q_{10} = 0.0886$	
$a_5 = 0.0353$	$q_{11} = 0.2616$	
$a_6 = 0.0405$	$q_{12} = 0.1734$	
$b_0 = 1.0000$	$q_{13} = 0.0178$	
$b_1 = -1.3166$	$q_{20} = 0.1513$	
$b_2 = 0.6631$	$q_{21} = 0.2550$	
	$q_{22} = 0.1012$	

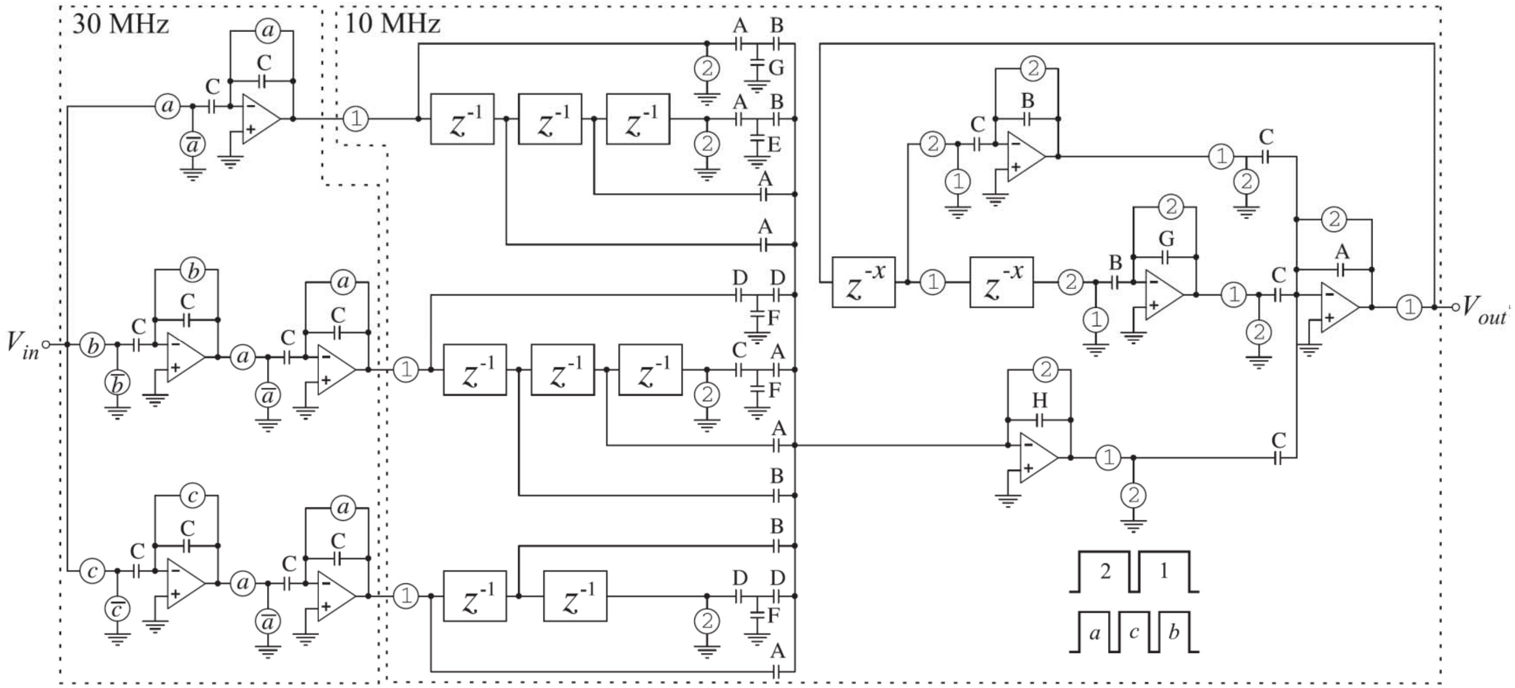
Efficient Decimation Filter Design

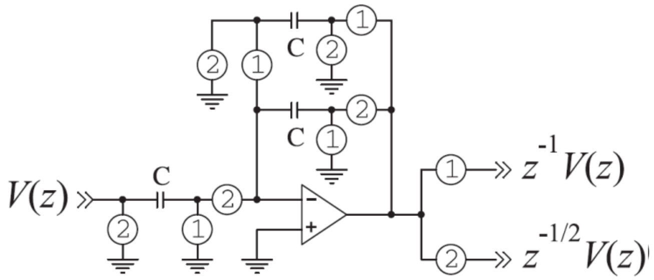
Block diagram of the decimation filter



Efficient Decimation Filter Design

Schematic diagram of the decimation filter

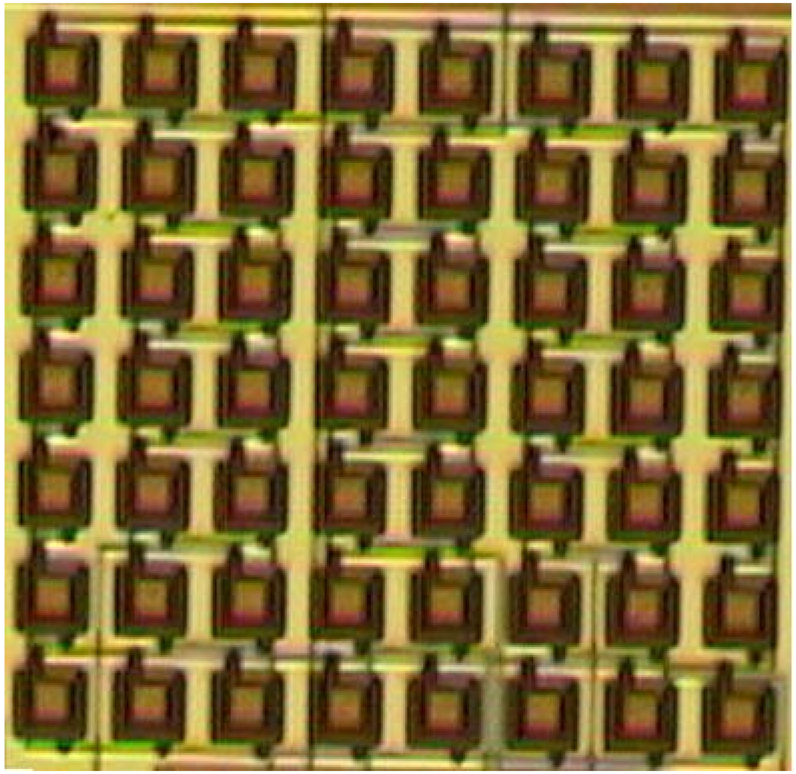




A = 0.2 pF	E = 0.7 pF
B = 0.3 pF	F = 0.8 pF
C = 0.1 pF	G = 0.9 pF
D = 0.4 pF	H = 1.2 pF

Efficient Decimation Filter Design

Capacitances are implemented by parallel associations of 0.1 pF, 5µmX5µm unit capacitors



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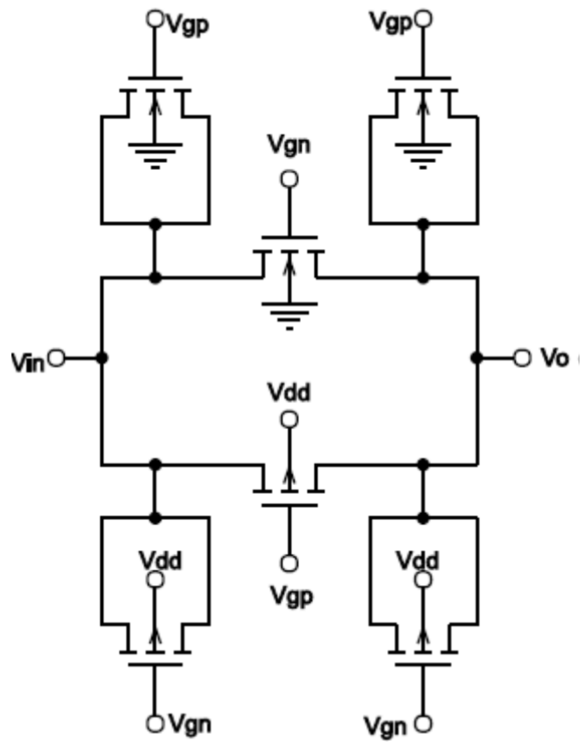
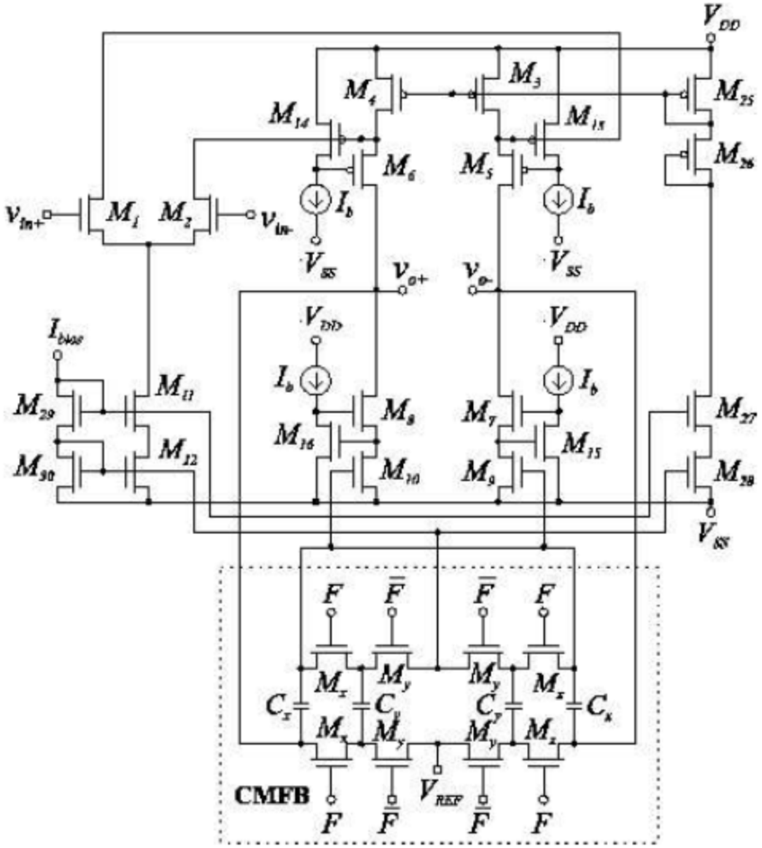
Efficient Decimation Filter Design

Switches are implemented with dummy transistors to reduce charge injection

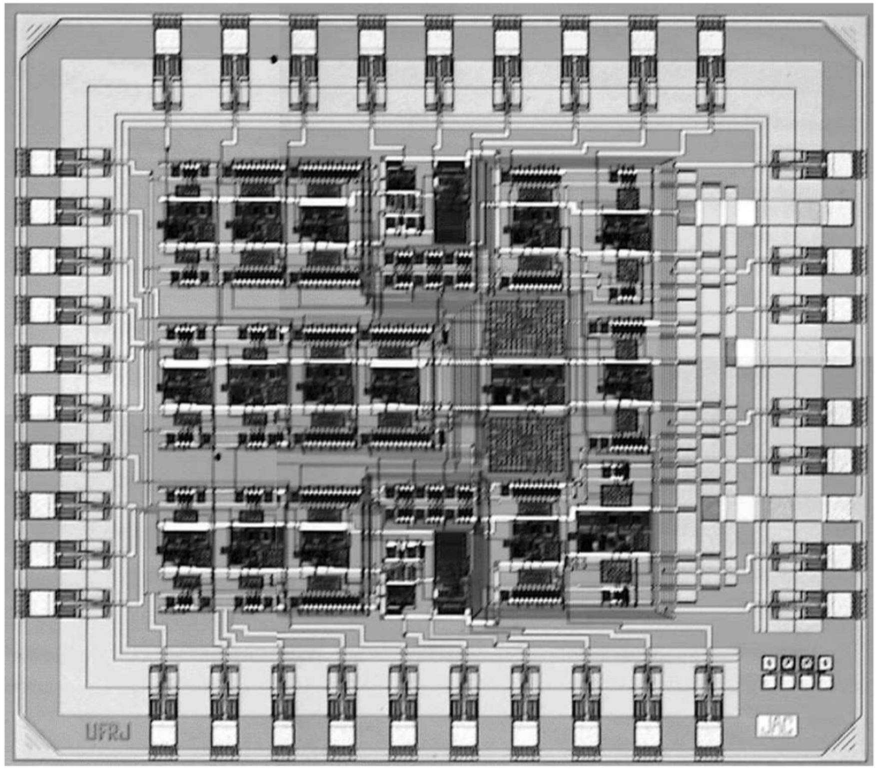


Efficient Decimation Filter Design

Operational transconductance amplifiers



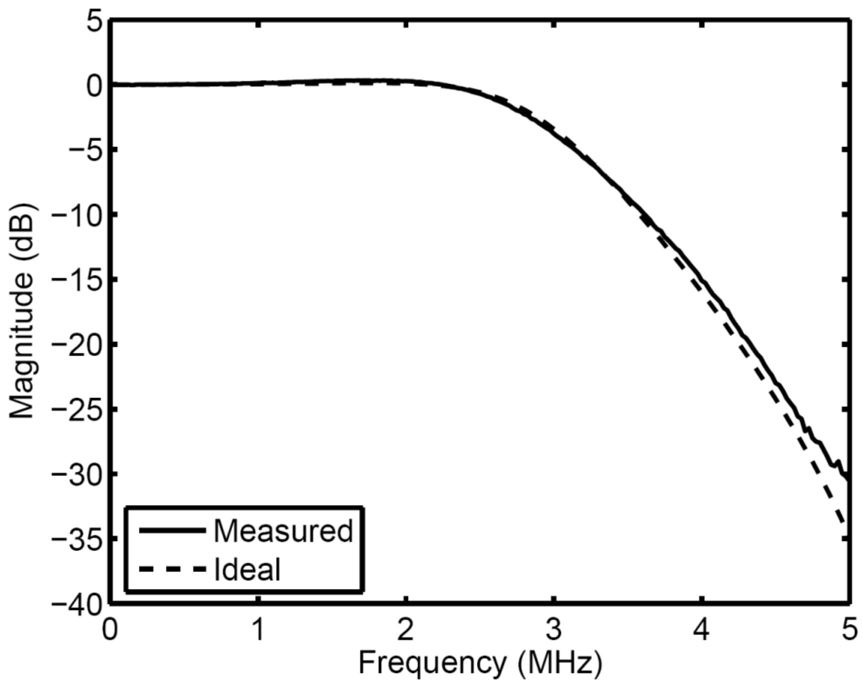
Efficient Decimation Filter Design



Chip photograph – Die area = 1.86 × 1.50 mm^2

Efficient Decimation Filter Design

Measured and ideal frequency responses



Voltage Supply	5V
Input Sampling Frequency	30 MHz
Output Sampling Frequency	10 MHz
Dynamic Range (1% THD)	58 dB
Dye Area	2.8 mm^2
Power Consumption	67.2 mW