Direct-Form SC Filters
Direct-Form FIR SC Filter Realization

(L-1)th-order FIR SC filter:

\[
\frac{V_{out}}{V_{in}}(z) = \sum_{k=0}^{L-1} g_k z^{-k}
\]
Direct-Form FIR SC Filter Realization

Ex.: 4th-order SC FIR filter

\[
\frac{V_{out}}{V_{in}}(z) = -\frac{C_0}{C_f} - \frac{C_1}{C_f}z^{-1} - \frac{C_2}{C_f}z^{-2} - \frac{C_3}{C_f}z^{-3} + \frac{C_4}{C_f}z^{-4}
\]
Reduction of the number of amplifiers by a multiplexing technique
Direct-Form IIR SC Filter Realization

Direct Form I
2 SC arrays sharing the same SC delay line

Ex.: \[
\frac{V_{out}}{V_{in}}(z) = \frac{a_0 + a_1 z^{-1} + \cdots + a_8 z^{-8}}{1 - b_1 z^{-1} - b_2 z^{-2}}
\]
Direct-Form IIR SC Filter Realization

Ex.: \[ \frac{V_{out}}{V_{in}}(z) = \frac{a_0 + a_1 z^{-1} + \cdots + a_8 z^{-8}}{1 - b_1 z^{-1} - b_2 z^{-2}} \]
Capacitors in CMOS Technology

\[ C = AC_{ox} \]
\[ C_{ox} = \varepsilon_{ox}/t_{ox} \]

For 0.35 \( \mu \)m CMOS:
\[ \varepsilon_{ox} \approx 3.5 \times 10^{-13} \text{ F/cm} \]
\[ t_{ox} \approx 10 \text{ nm} \]
\[ \Rightarrow C_{ox} \approx 3.5 \text{ fF/\( \mu \)m}^2 \]
**Capacitance Ratio Error Sources**

**Very small capacitors:**
- The actual capacitance ratio can be significantly different from unity.

\[ \text{fabricated capacitor} \]
\[ \text{intended capacitor} \]

**Large capacitors:**
- Better ratio accuracy;
- However, if the plates are too large: (i) chip area may be excessive; (ii) opposite regions of the two capacitors may be affected differently by the fabrication process (e.g., slight difference in oxide thickness $t_{\text{ox}}$);
Systematic error caused by overetching:

- Occurs when the upper layer of polysilicon or metal is being etched;
- The relative area error of two capacitors will be the same if their nominal perimeter/area ratio is the same;
- Therefore the capacitance ratio will not be affected.
Overetching effects

Let \( A'_1 = (x_1 - 2\Delta l)(y_1 - 2\Delta l) \)
\[ \approx x_1 y_1 - 2(x_1 + y_1)\Delta l \]
\[ = A_1 - P_1 \Delta l \]

The relative area error is
\[ \frac{\Delta A_1}{A_1} = -\frac{P_1 \Delta l}{A_1} \]

The real capacitance ratio is
\[ \frac{C'_1}{C'_2} = \frac{A'_1}{A'_2} = \frac{A_1 \left(1 - \frac{P_1 \Delta l}{A_1}\right)}{A_2 \left(1 - \frac{P_2 \Delta l}{A_2}\right)} \]

Therefore, if
\[ \frac{P_1}{A_1} = \frac{P_2}{A_2} \]
then
\[ \frac{C'_1}{C'_2} = \frac{C_1}{C_2} \]
Techniques to improve capacitance ratio accuracy:

– Parallel connection of identical unit capacitors to implement each capacitance
  => Systematic error is compensated;
– Arrangement of unit capacitors in common centroid layout;
– Careful routing inside capacitor matrices.

Unit capacitor: $C = 100 \text{ fF}$

$A = 5\mu\text{m} \times 5\mu\text{m}$
Capacitor Layout

Process technology: 0.35 μm CMOS
Dimensions: 3.2 x 0.90 mm²
Unit capacitance: 100 fF
Parasitic Capacitances

crossover capacitances

crosstalk capacitances
Parasitic Capacitances
Mismatch Caused by Process Gradients

Symmetrical layout with common centroid: evaluation of the mean capacitance of each capacitor, assuming a linear model for $t_{ox}$ variation:

\[
\langle C_{xy} \rangle_A = \frac{1}{16} \cdot [16 C_u + 48 \alpha + 32 \beta] = C_u + 3 \alpha + 2 \beta
\]

\[
\langle C_{xy} \rangle_B = \frac{1}{14} \cdot [14 C_u + 42 \alpha + 28 \beta] = C_u + 3 \alpha + 2 \beta
\]

\[
\langle C_{xy} \rangle_C = \frac{1}{4} \cdot [4 C_u + 12 \alpha + 8 \beta] = C_u + 3 \alpha + 2 \beta
\]

\[
\langle C_{xy} \rangle_D = C_u + 3 \alpha + 2 \beta
\]
Mismatch Caused by Process Gradients

Asymmetrical layout with common centroid:

\[
\langle C_{xy} \rangle_A = \frac{1}{16} \cdot [16 C_u + 48 \alpha + 32 \beta] = C_u + 3 \alpha + 2 \beta
\]

\[
\langle C_{xy} \rangle_B = \frac{1}{14} \cdot [14 C_u + 42 \alpha + 28 \beta] = C_u + 3 \alpha + 2 \beta
\]

\[
\langle C_{xy} \rangle_C = \frac{1}{4} \cdot [4 C_u + 12 \alpha + 8 \beta] = C_u + 3 \alpha + 2 \beta
\]

\[
\langle C_{xy} \rangle_D = C_u + 3 \alpha + 2 \beta
\]
Mismatch Caused by Process Gradients

Difficulties:
– Common centroid arrangement is not a simple task when the number of capacitance ratios is large;
– Common centroid layout is not always possible;
– When it is possible, there are several alternatives.

Solutions(*):
– Common centroid layout tends to increase the spatial correlation coefficients of the capacitors;
– Find the optimal arrangement that minimizes the common centroid error and maximizes the spatial correlation.

Capacitance Mismatch Effects

Mathematical model commonly used in computer aided analysis of SC filters:

\[ \hat{\gamma}_k = \gamma_k + \epsilon_{\gamma_k} \]

were \( \epsilon_{\gamma_k} = \gamma_k \epsilon_k \)

\( \gamma_k \) : desired capacitance ratios

\( \epsilon_k \) : uncorrelated zero-mean Gaussian random variables
Capacitance Mismatch Effects

Ex.: Frequency responses of 3 FIR filters having $L = 50$ and $\sigma_\epsilon = 0.001$
Capacitance Mismatch Effects

a) FIR SC Filters(*)

\[ G(e^{j\omega}) = \sum_{k=0}^{L-1} g_k e^{-j\omega k} \]

Each coefficient is implemented as a ratio between two capacitances

Because of random capacitance errors, the actual frequency response is:

\[ \hat{G}(e^{j\omega}) = \sum_{k=0}^{L-1} (g_k + \epsilon g_k) e^{-j\omega k} \]

\[ = G(\omega) + \sum_{k=0}^{L-1} \epsilon g_k e^{-j\omega k} \]

Capacitance Mismatch Effects

Deviation in the frequency response:

$$
\Delta G(e^{j\omega}) = \hat{G}(e^{j\omega}) - G(e^{j\omega}) = \sum_{k=0}^{L-1} \epsilon_{g_k} e^{-j\omega k}.
$$

where \( \epsilon_{g_k} = \overline{g} \epsilon_k \) and \( \overline{g} = \frac{\sum_{k=0}^{L-1} |g_k|}{L} \)

(i) \( \epsilon_k \) are random Gaussian mismatches in unit capacitance arrays, with zero mean and standard deviation \( \sigma_\epsilon \)

(ii) \( |\Delta G(e^{j\omega})| \) is a Rayleigh random variable with a mean (average) value

$$
|\Delta G(e^{j\omega})| = \sigma_g \sqrt{\pi L}, \quad \forall \omega
$$

where \( \sigma_g = \overline{g} \sigma_\epsilon \)
b) IIR SC Filters (*)

\[ H(z) = \frac{A(z)}{B(z)} = \frac{\sum_{k=0}^{M-1} a_k z^{-k}}{1 - \sum_{k=1}^{N-1} b_k z^{-k}} \]

Each coefficient is implemented as a ratio between two capacitances

The average deviation in frequency response is:

\[ |\Delta H|_{e^{j\omega}} = \begin{cases} 
\frac{\sigma_b \sqrt{\pi(N-1)}}{2|B(e^{j\omega})|}, & \omega \in \Omega_p \\
\frac{\sigma_a \sqrt{\pi M}}{2|B(e^{j\omega})|}, & \omega \in \Omega_s 
\end{cases} \]

where \( \sigma_a = \sigma_c \sum_{k=0}^{M-1} \frac{|b_k|}{M} \), \( \sigma_b = \sigma_c \sum_{k=1}^{N-1} \frac{|b_k|}{(N-1)} \)

Letting $z_1, z_2, ..., z_{N-1}$ be the poles of $H(z)$:

$$|B(e^{j\omega})| = |e^{j\omega} - z_1||e^{j\omega} - z_2|...|e^{j\omega} - z_{N-1}|$$
Capacitance Mismatch Effects

Example: $\omega_p = 0.2; \omega_s = 0.3; R_p < 1\text{dB}; R_s > 60\text{ dB}$

--- Elliptic: $M=N=6$
__ Two-pole design: $M=9, N=3$
__. FIR: $M=22, N=1$
Capacitance Mismatch Effects

Elliptic:
M=N=6

Two-pole design:
M=9, N=3