Chaves e Capacitores

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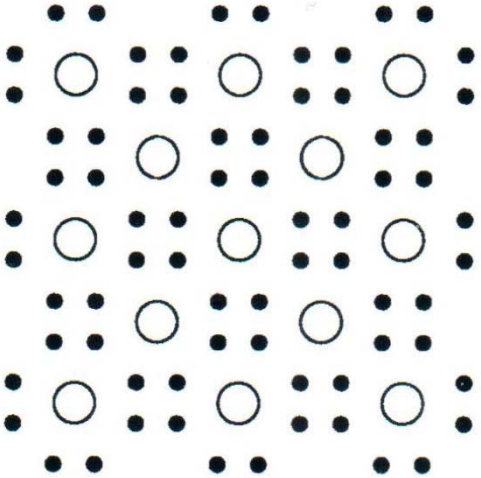
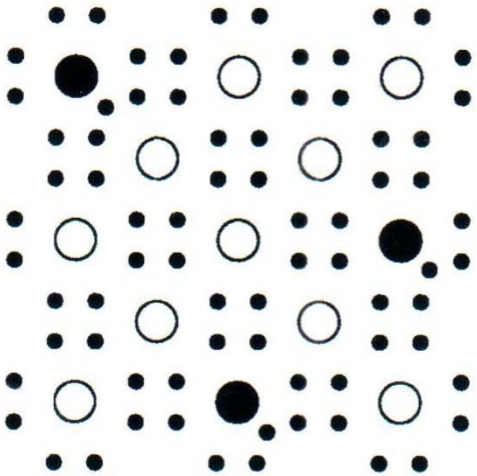
Dopagem

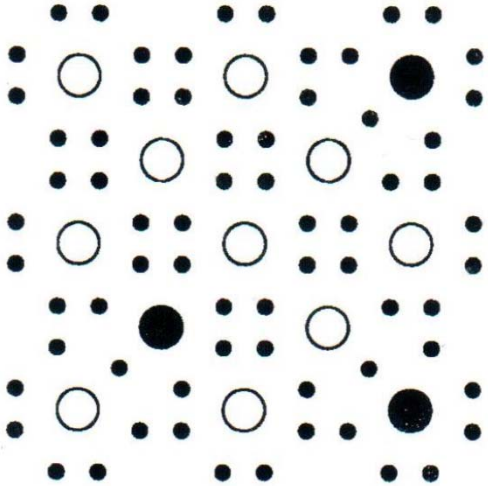


Silício puro:
4 elétrons na camada de valência



Silício dopado com fósforo: 5 elétrons na camada de valência

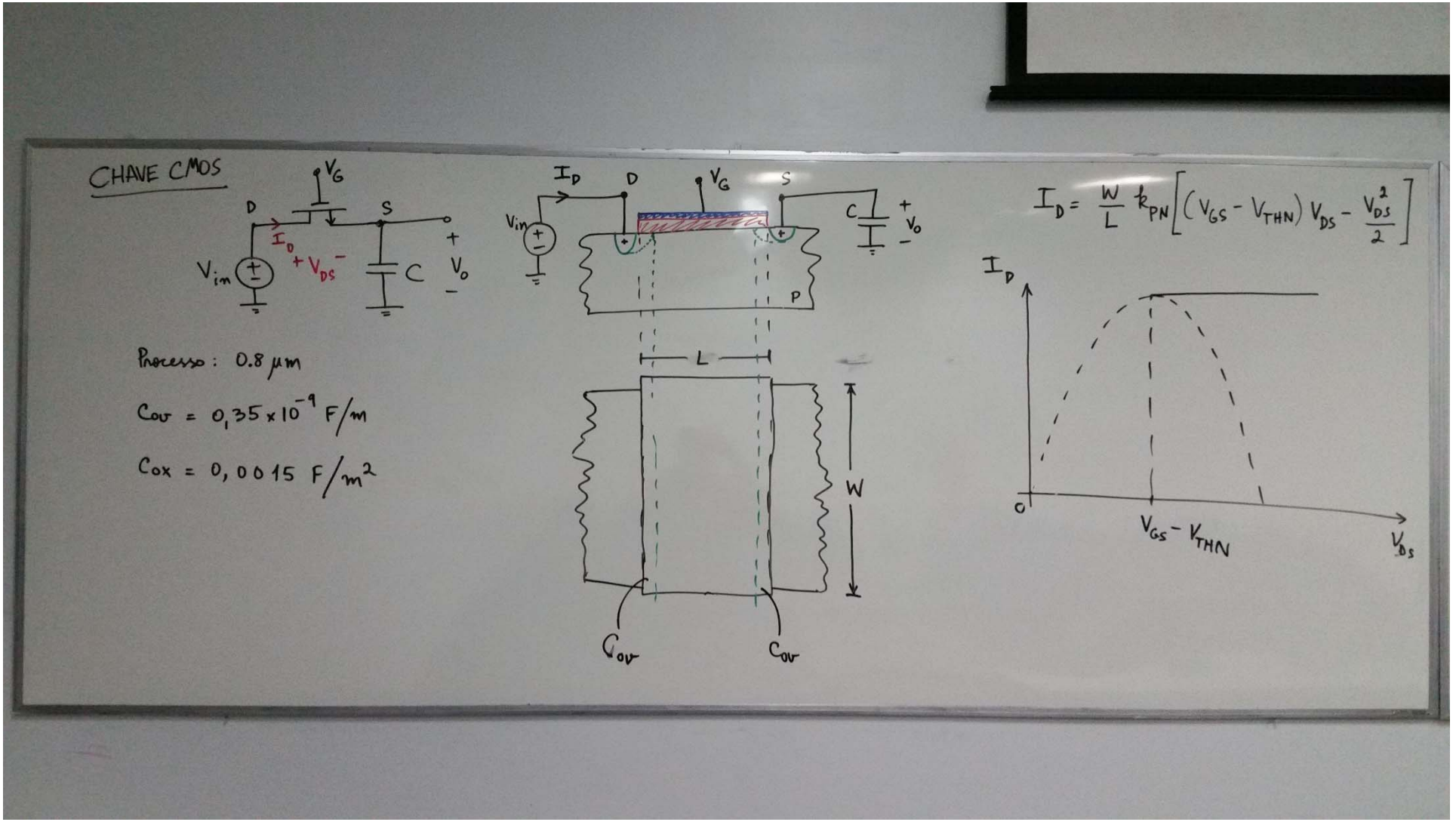
Semicondutor tipo *n*



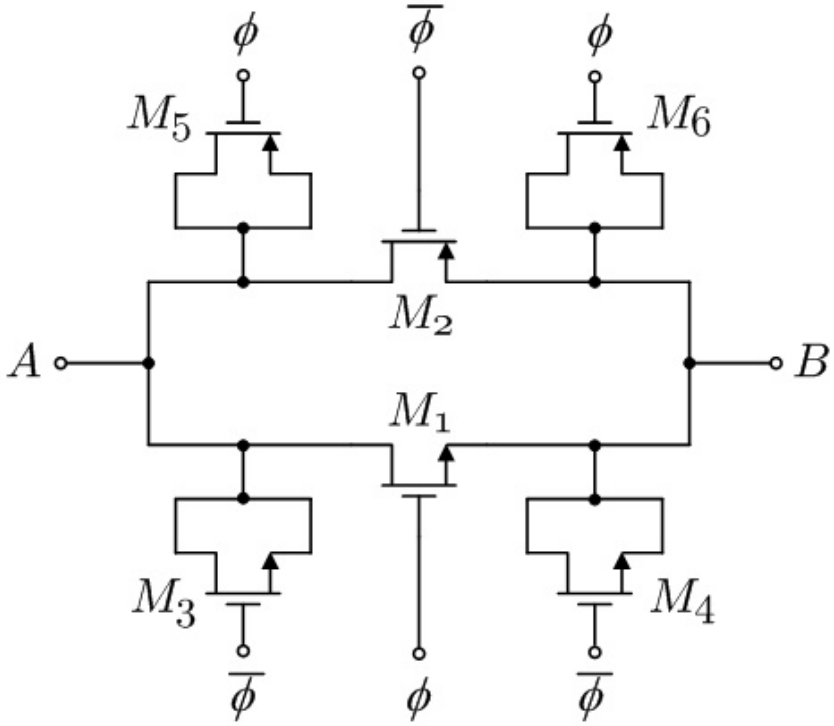
Silício dopado com boron: 3 elétrons na camada de valência

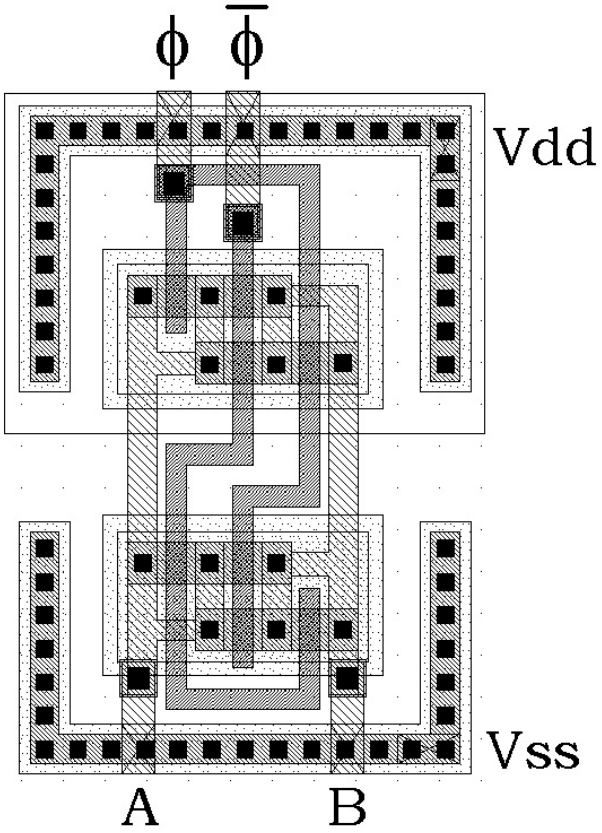
Semicondutor tipo *p*

Chave CMOS


CHAVE CMOS
V_G
D
S
I_D
$+ V_{DS} -$
V_{in}
C
$+ V_o -$
Processo: 0.8 μm
$C_{ov} = 0,35 \times 10^{-9}$ F/m
$C_{ox} = 0,0015$ F/m²
I_D
D
V_G
S
V_{in}
C
$+ V_o -$
P
L
W
C_{ov}
C_{ov}
$I_D = \frac{W}{L} k_{PN} \left[(V_{GS} - V_{THN}) V_{DS} - \frac{V_{DS}^2}{2} \right]$
I_D
0
$V_{GS} - V_{THN}$
V_{DS}

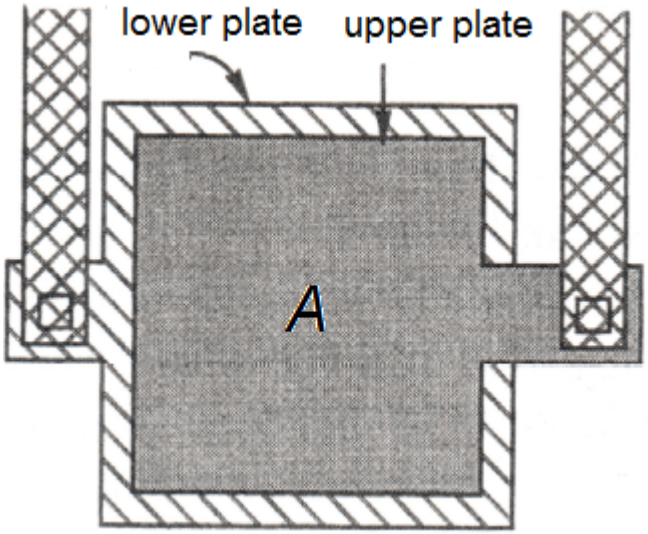
Chave CMOS

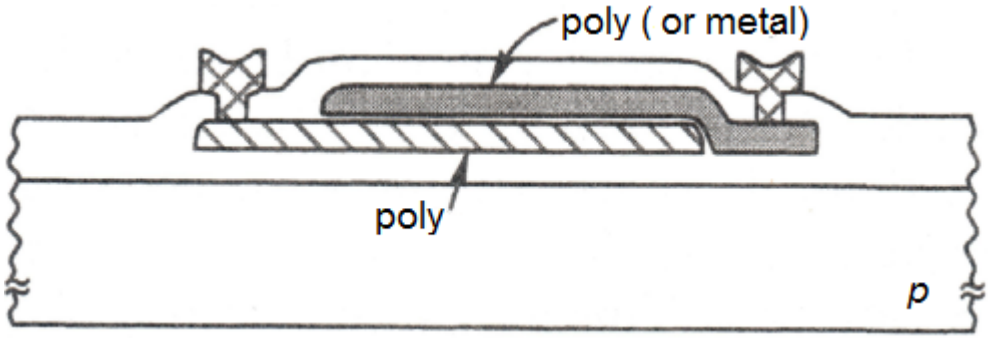




Dimensões: 11,5 µm x 15,2 µm

Capacitores em Tecnologia CMOS





$C = AC_{ox}$

$C_{ox} = \varepsilon_{ox}/t_{ox}$

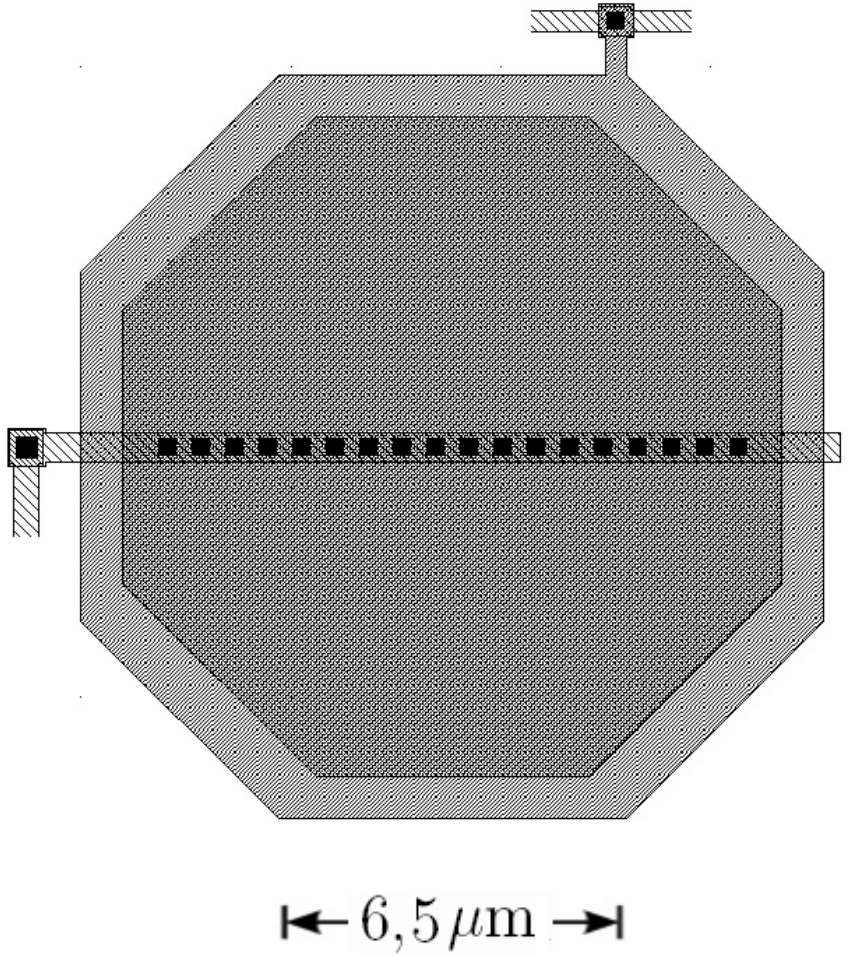
$\varepsilon_{ox} \approx 3.5 \times 10^{-13}$ F/cm

$t_{ox} \approx 10$ nm

$C_{ox} \approx 1.5$ fF/(μm)^2

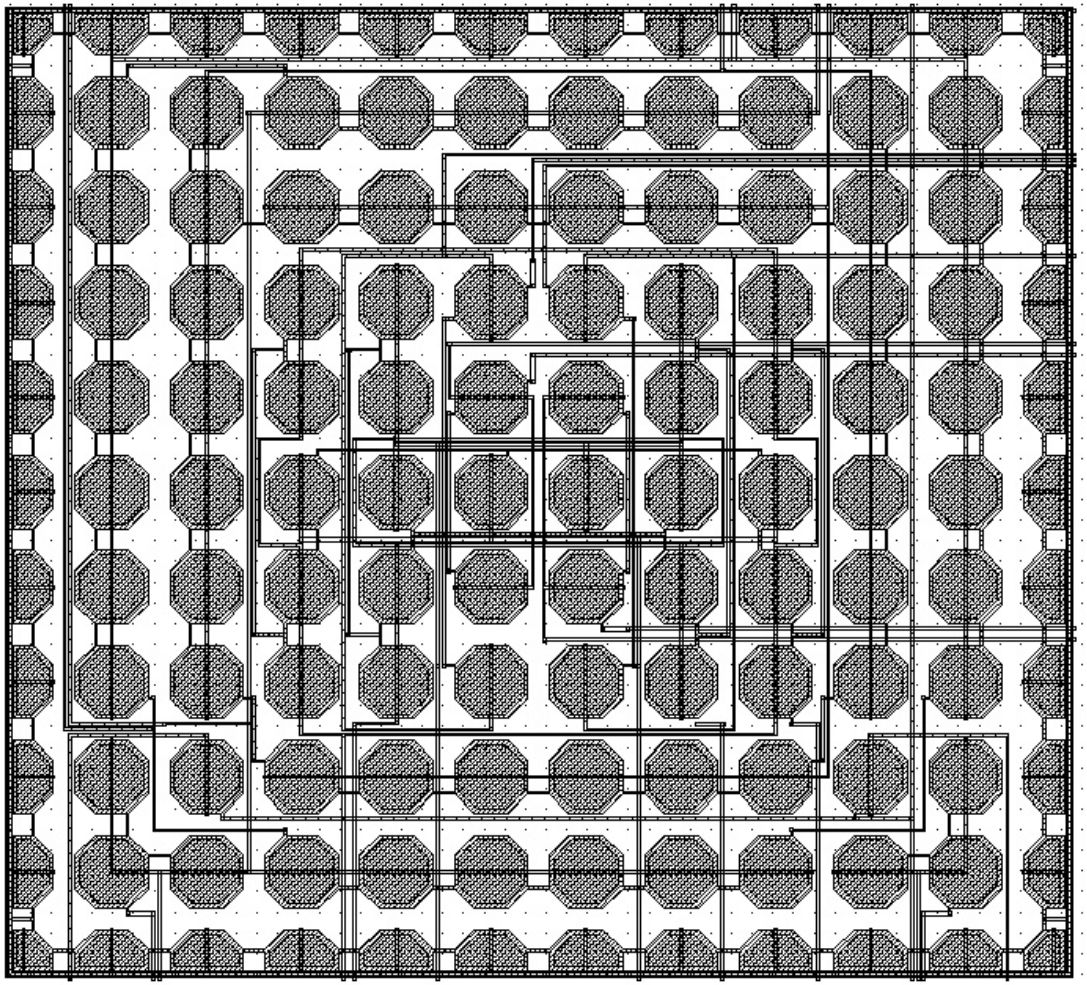
Processo: 0.8 μm

Capacitores

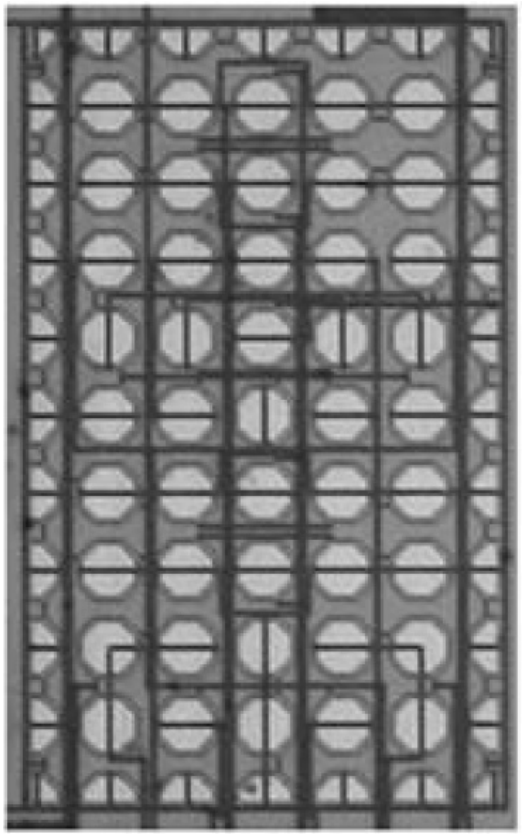


C = 200 fF

Layout de Matrizes de Capacitores



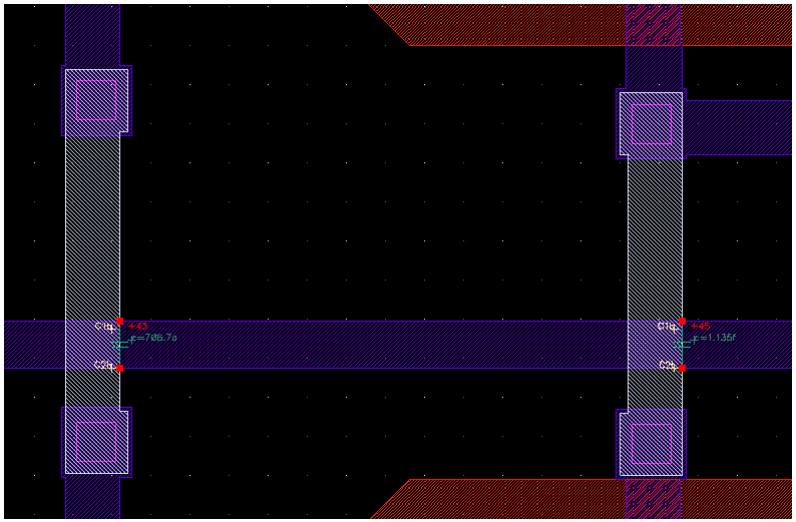
Desenho

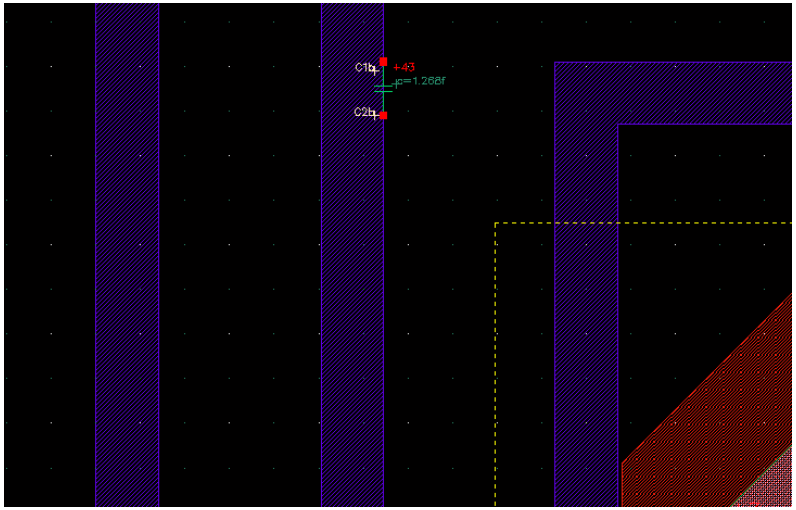


Fotografia

Capacitâncias Espúrias

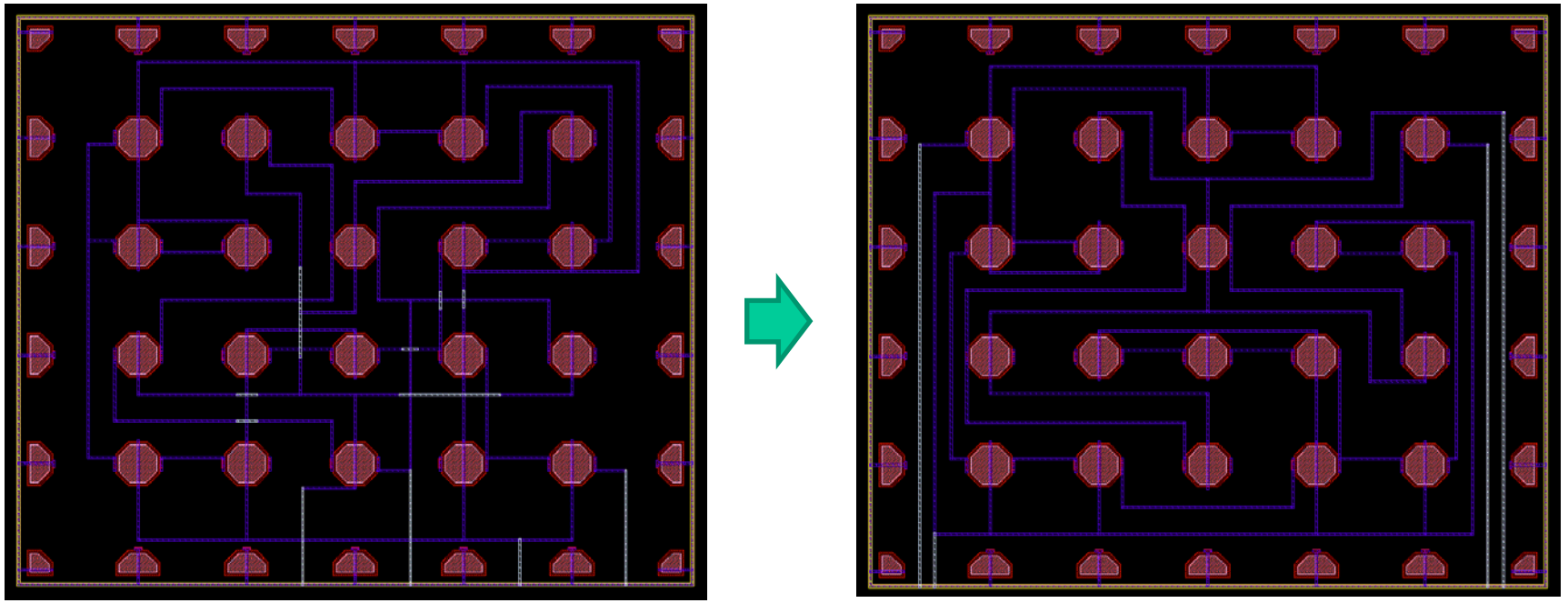
Capacitâncias de *Crossover*





Capacitâncias de *Crosstalk*

Melhorias no Layout



Melhorias no Layout