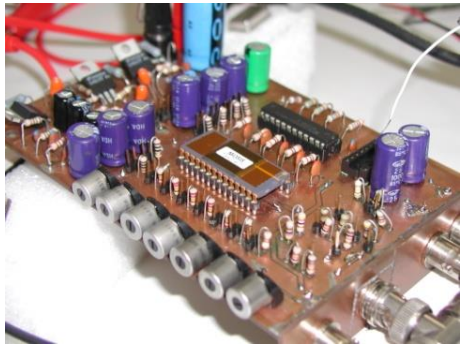
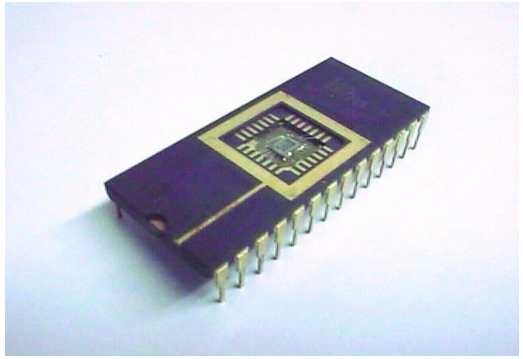
Introdução

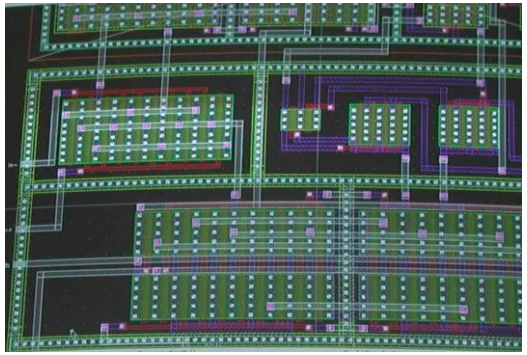
Laboratório de Processamento Analógico e Digital de Sinais (PADS/UFRJ)

Infraestrutura

- Equipamentos de teste em frequências desde DC até rádio-frequências.
- Licenças *Cadence* para o fluxo completo de projeto de circuitos integrados (CI´s): simulação, layout, DRC (design rule check), LVS (layout versus schematic).
- Acesso a foundries para fabricação de protótipos.







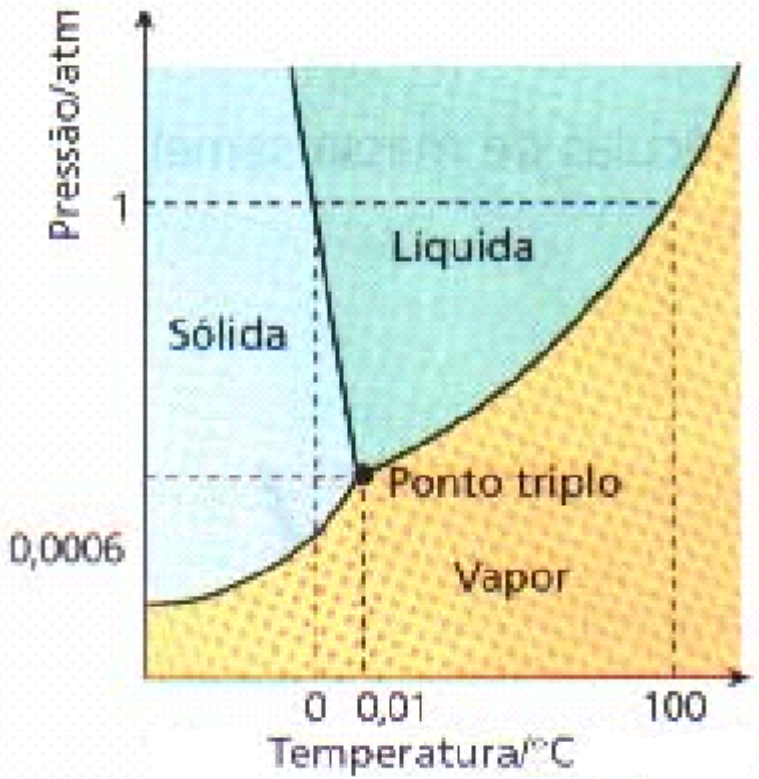
Exemplo de Projeto

Detecção do Efeito de Cavitação em Máquinas Hidroelétricas

Turbina Avariada

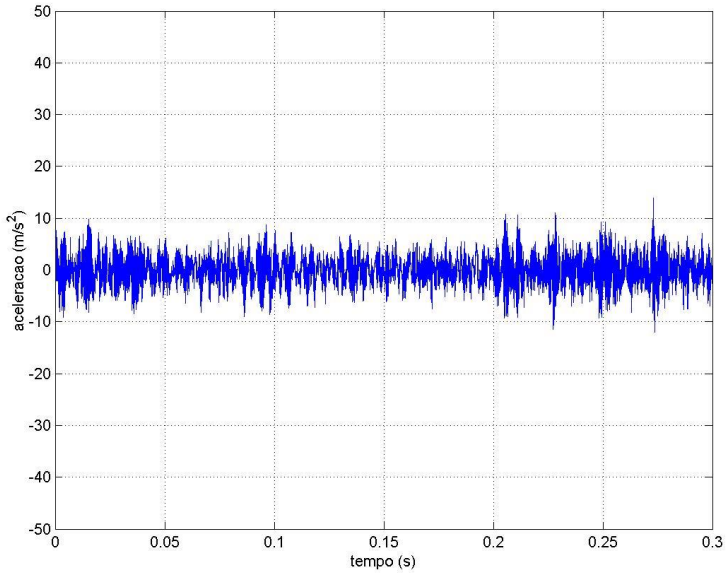
Turbina Recuperada

Como ocorre a cavitação ?

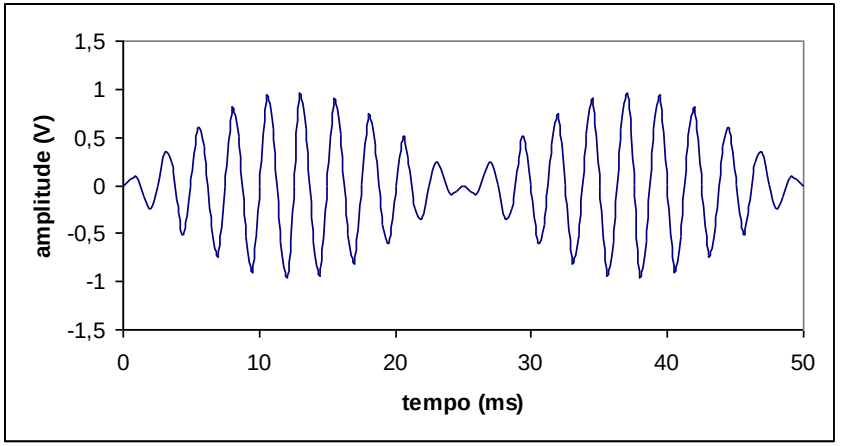


Detecção da Cavitação

Detecção da Cavitação

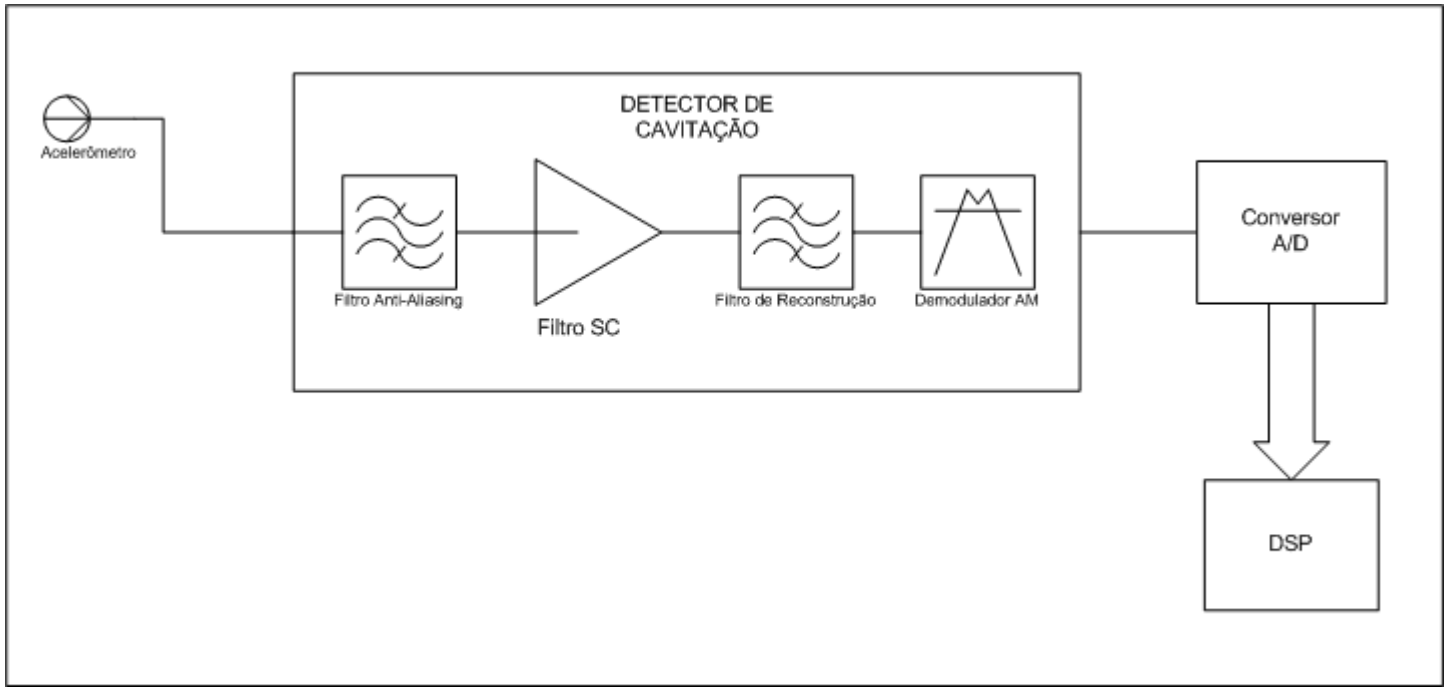


Sinal elétrico produzido pelo acelerômetro



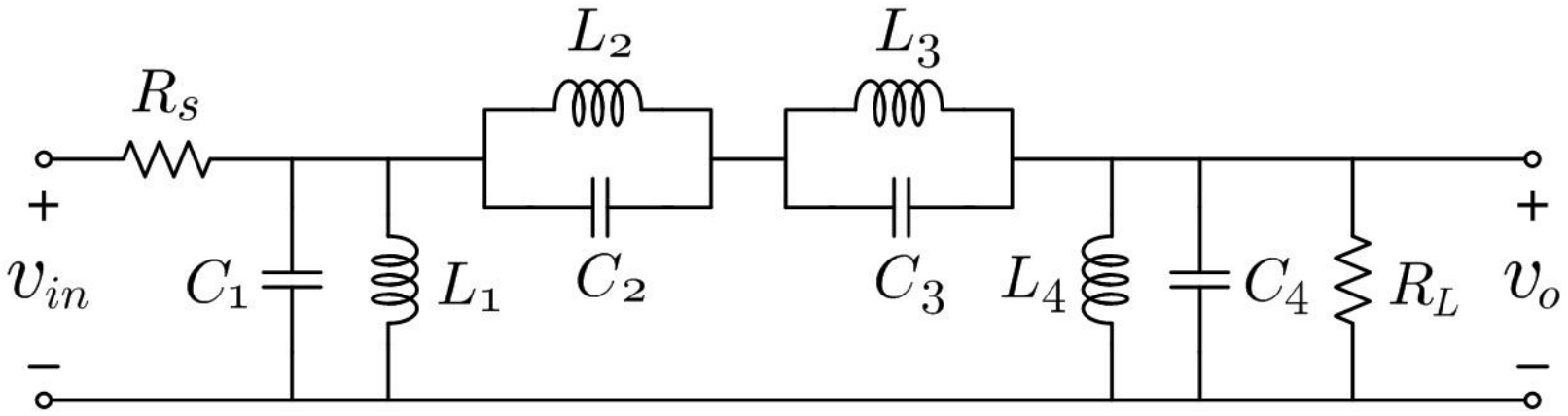
Sinal de interesse

Detecção da Cavitação

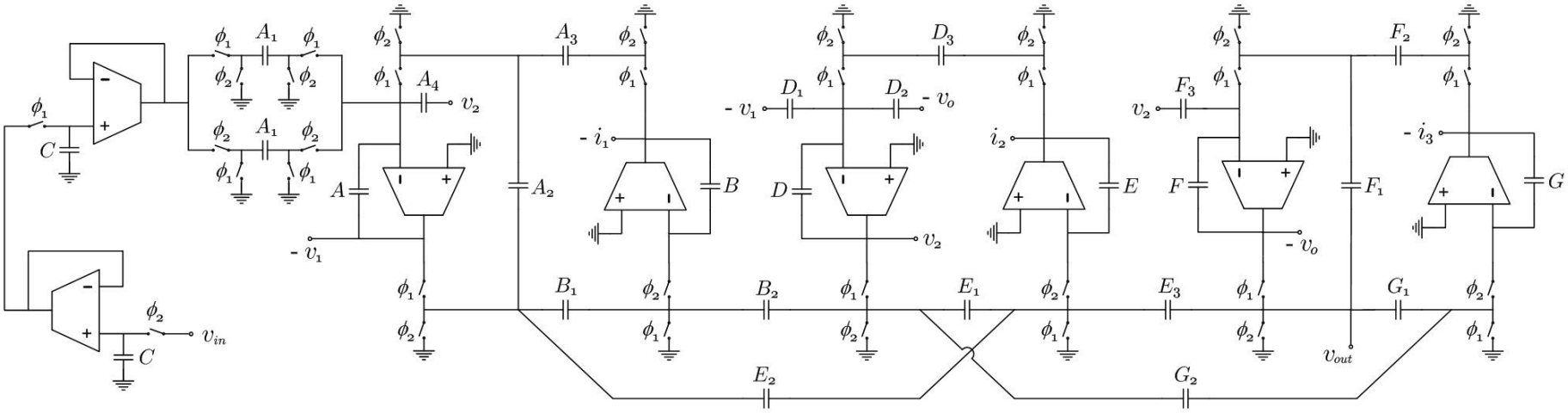


Eficiente combinação de técnicas microeletrônicas (semicondutores) e processamento digital de sinais (software).

Circuito do Filtro

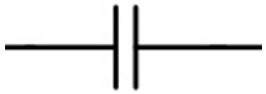


Circuito do Filtro com Componentes Microeletrônicos

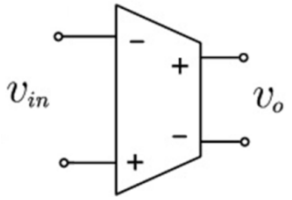


Componentes Básicos do Circuito do Filtro

- Capacitores

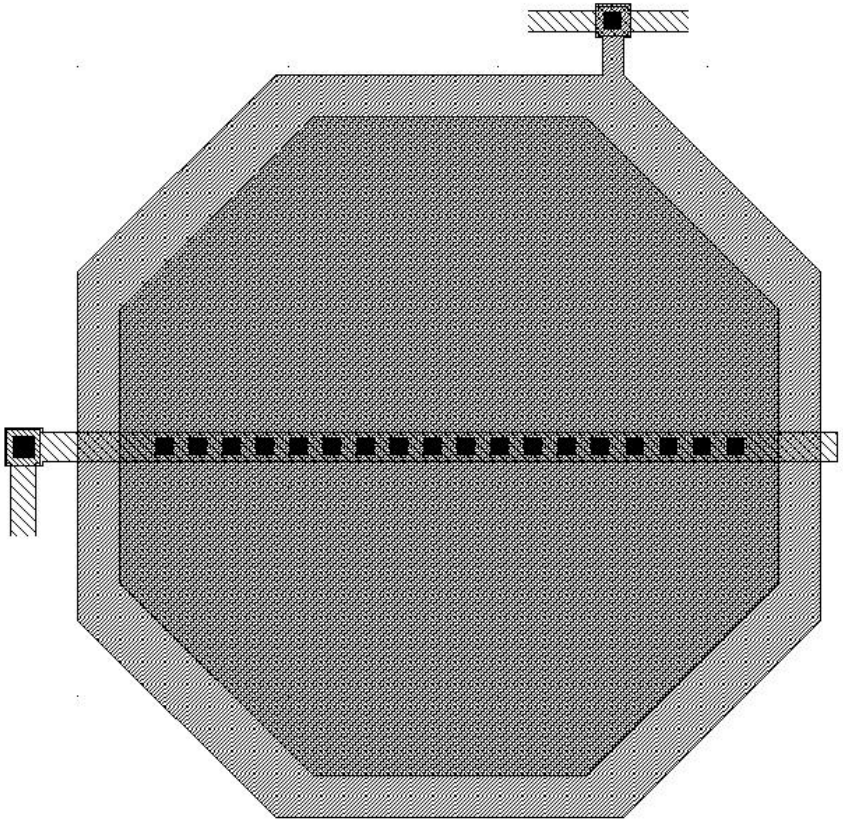


- Amplificadores



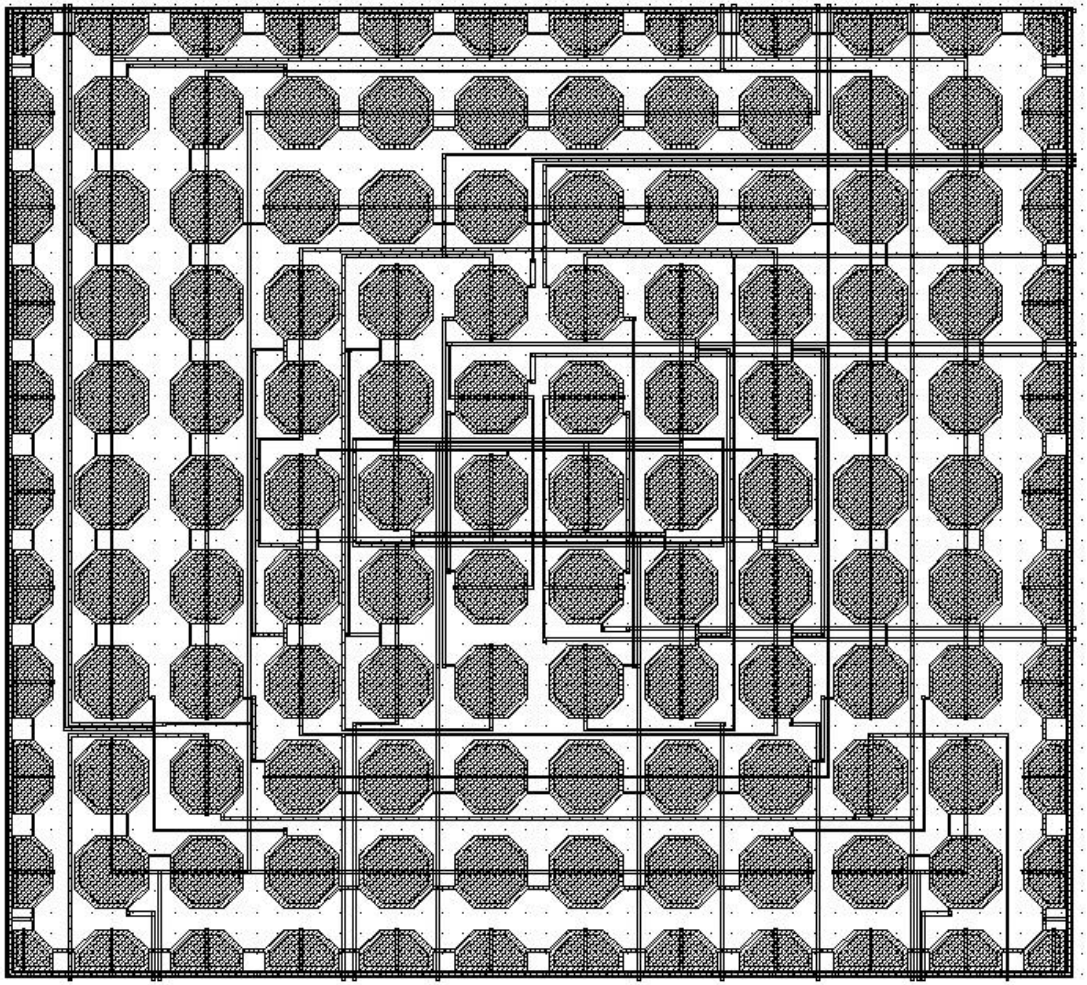
- Chaves Analógicas

Capacitores

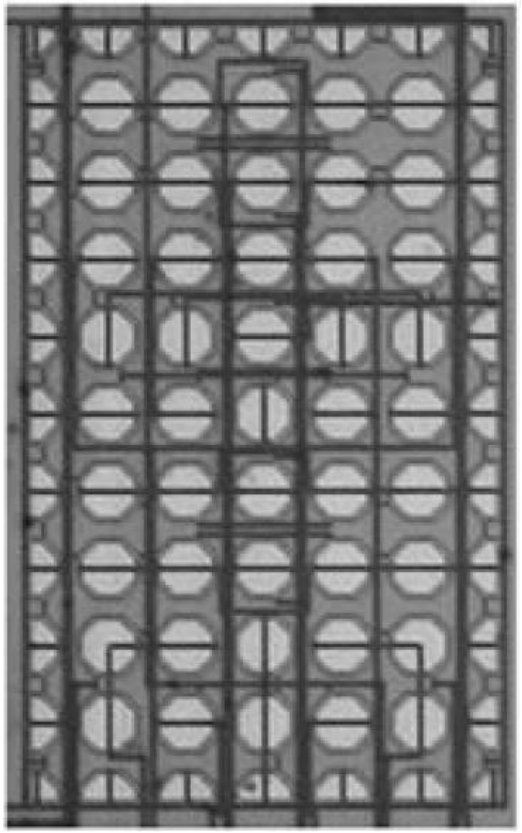


C = 200 fF

Layout de Matrizes de Capacitores

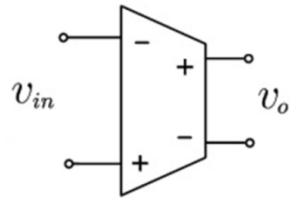


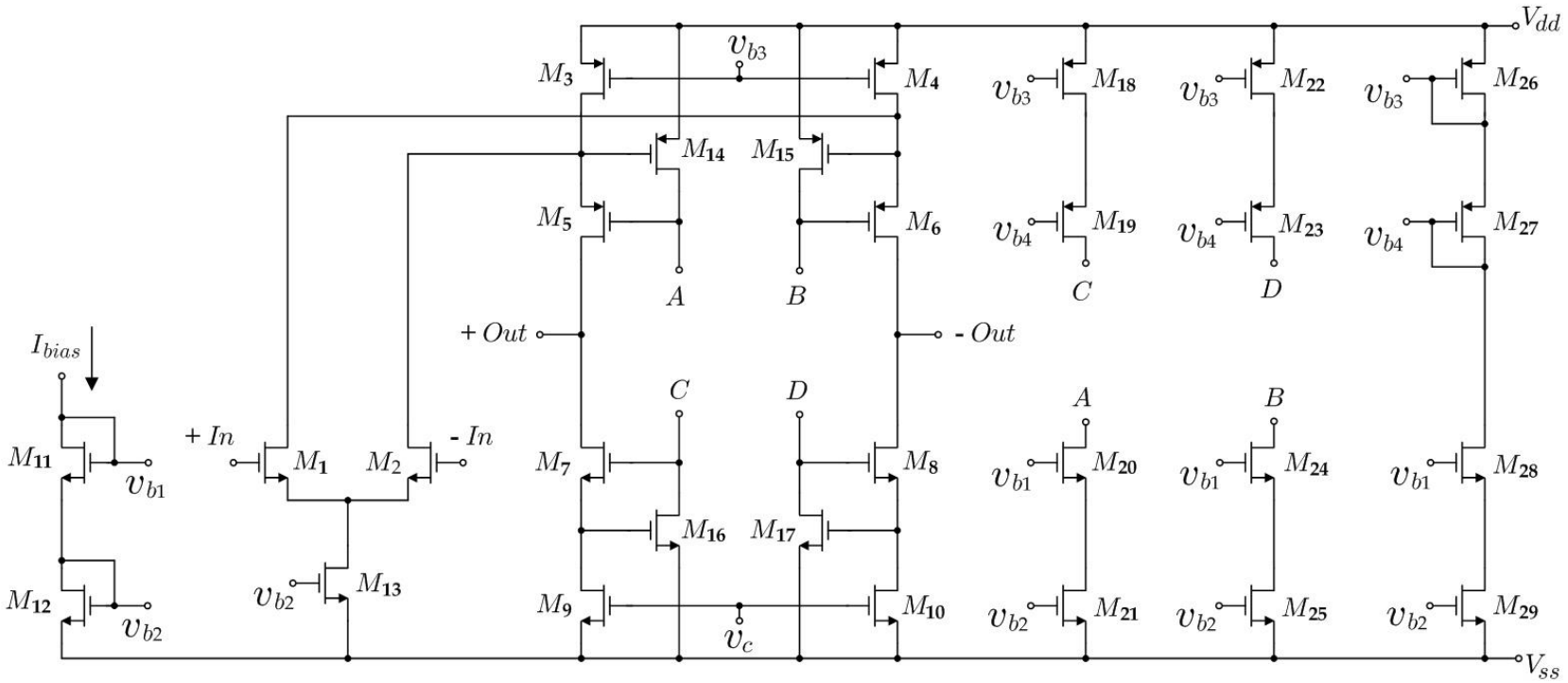
Desenho



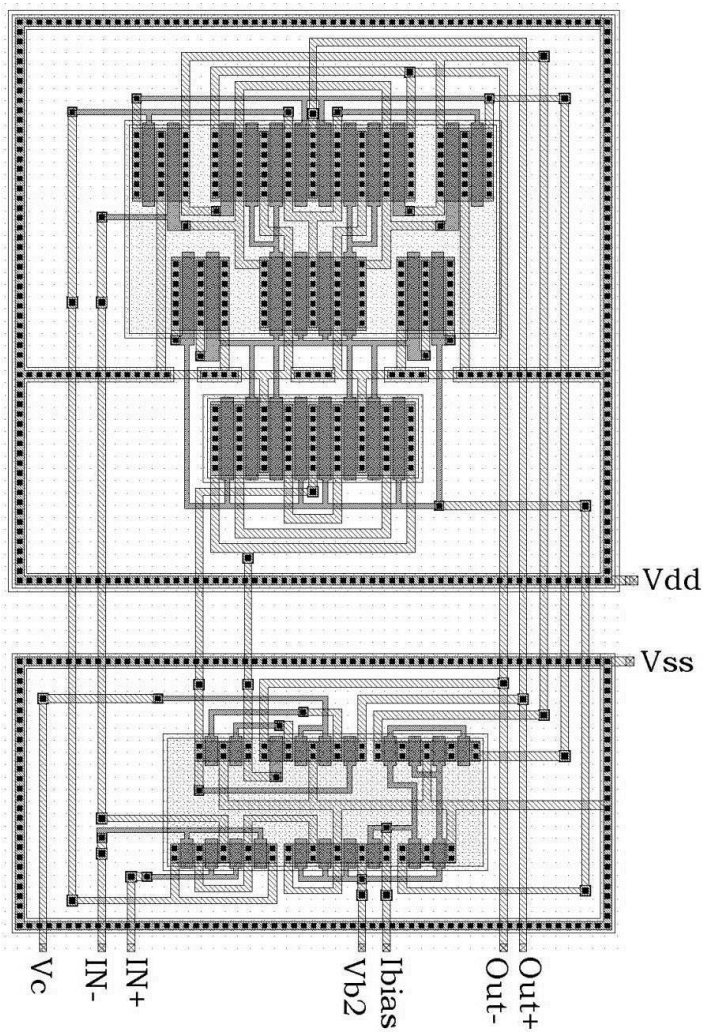
Fotografia

Amplificadores



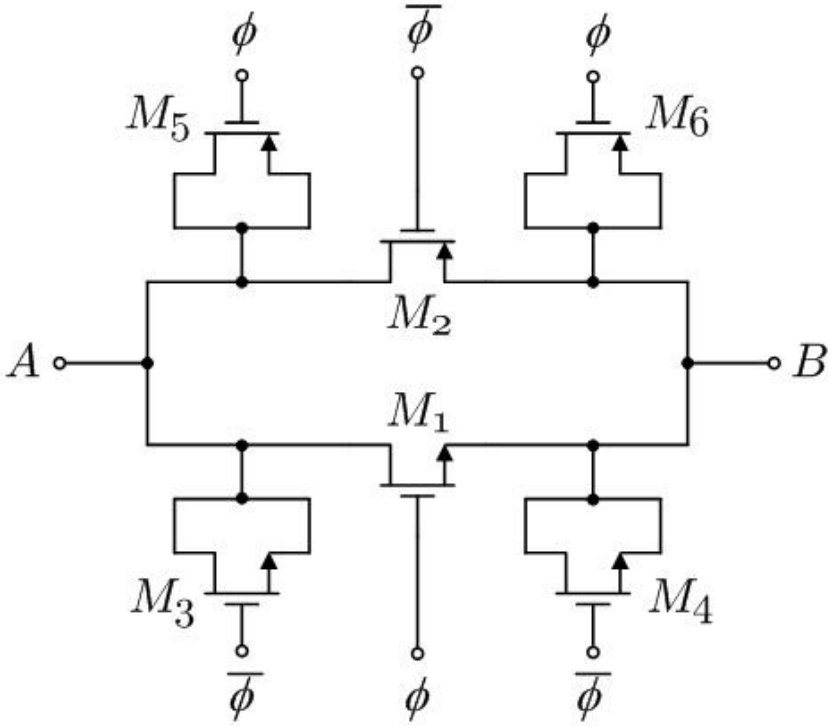


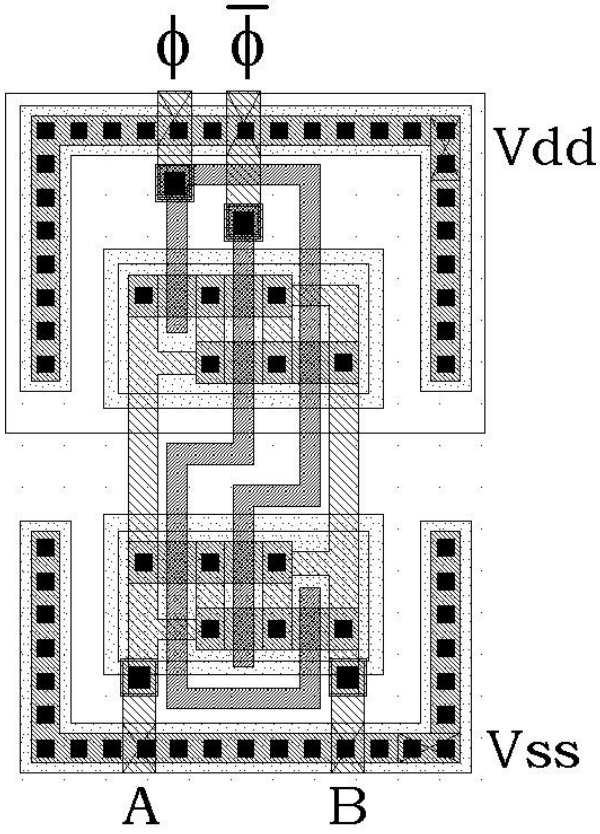
Layout dos Amplificadores



Dimensões: 49,9 μm x 76,2 μm

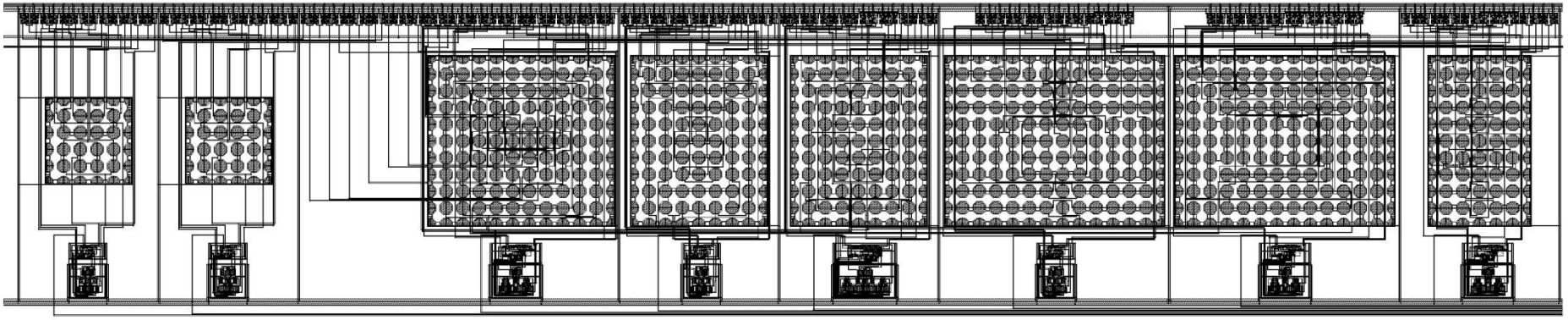
Chaves Analógicas





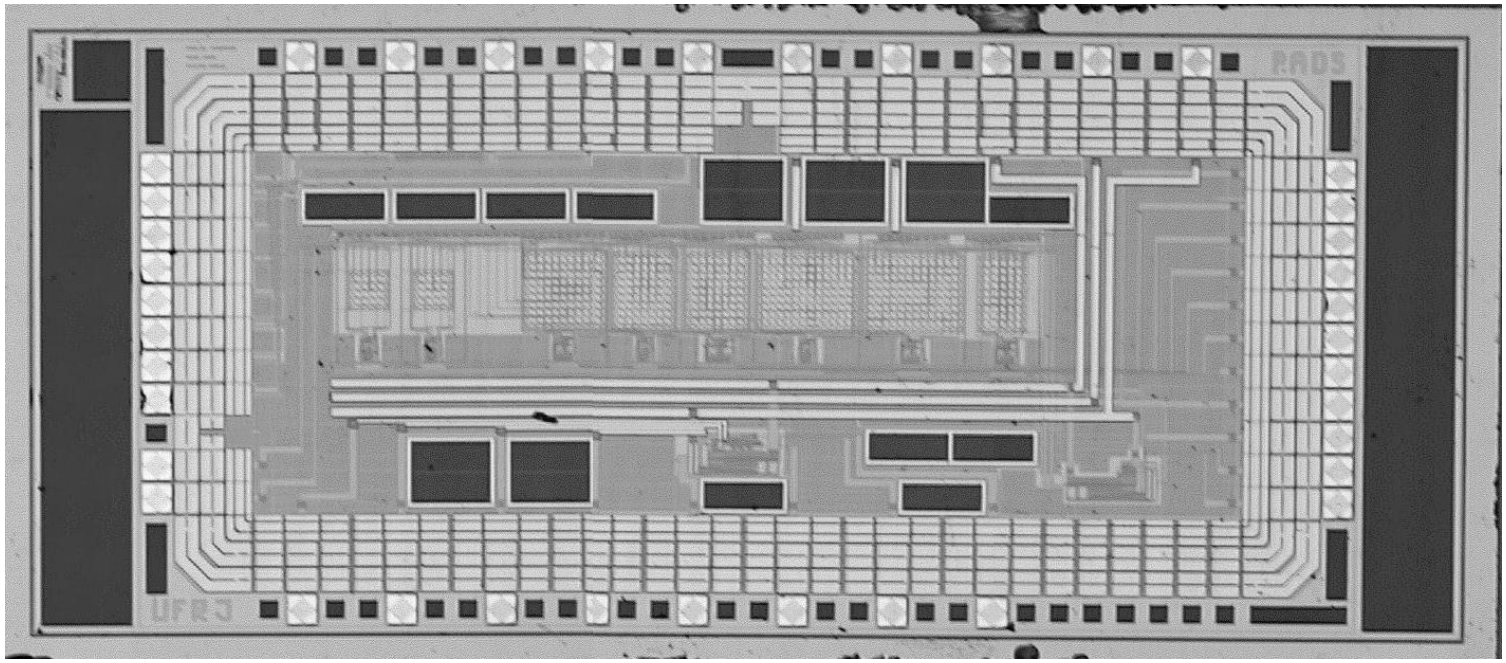
Dimensões: 11,5 μm x 15,2 μm

Layout do Circuito Completo

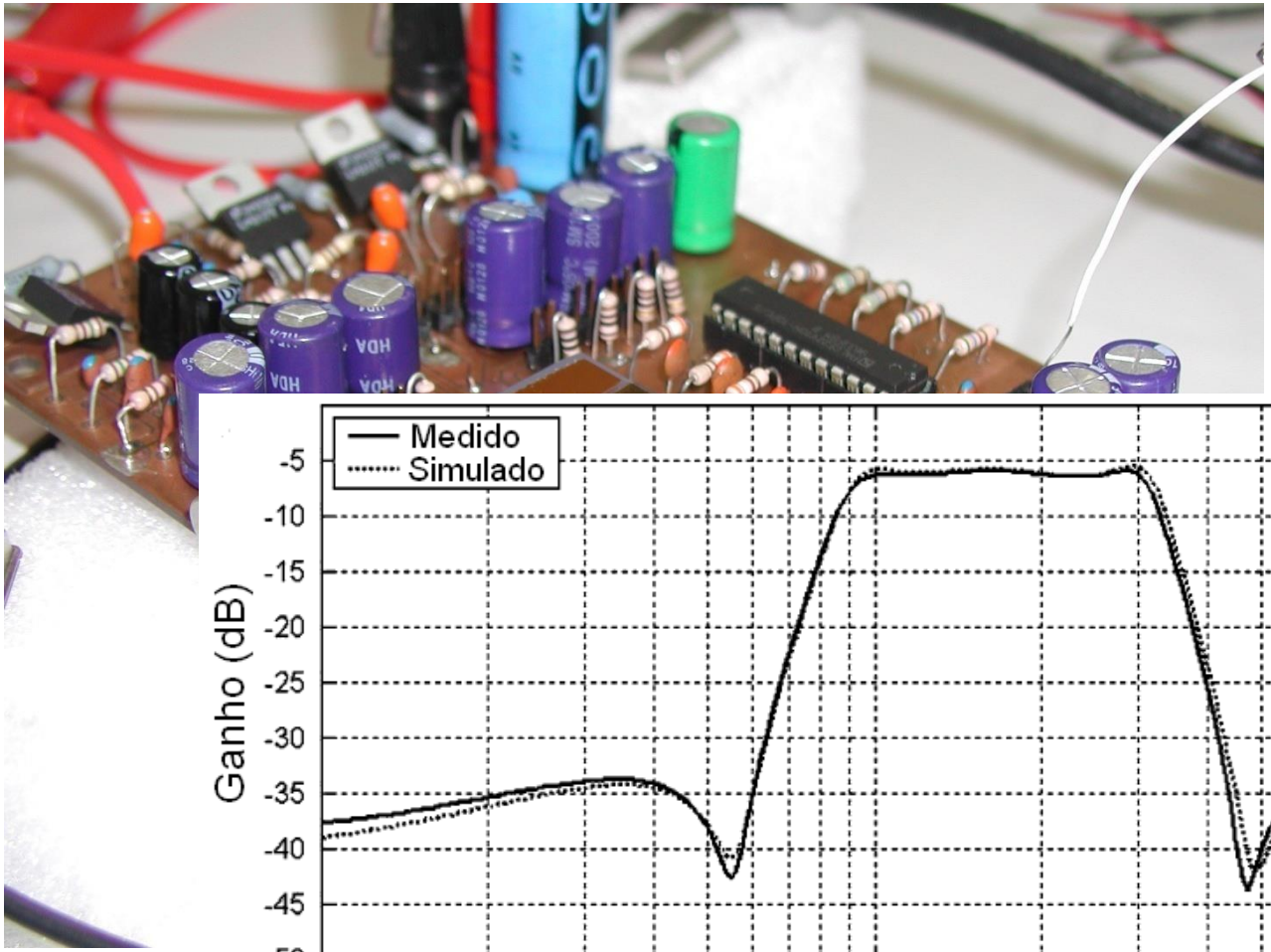


Dimensões: 2.3 mm x 0.49 mm

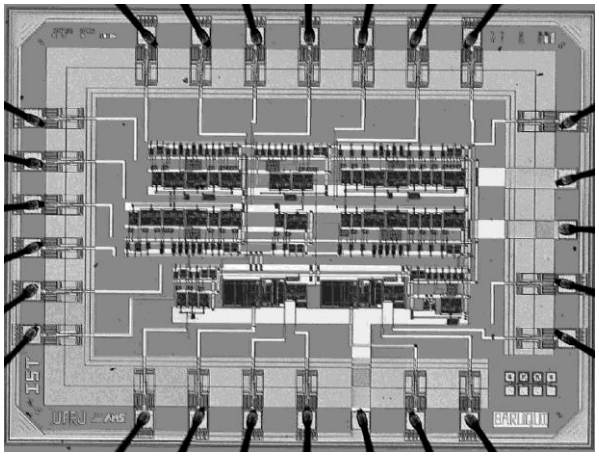
Fotografia do Circuito Integrado



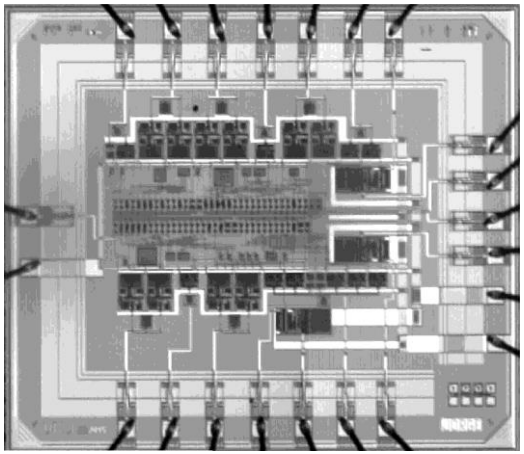
Teste do Circuito Integrado



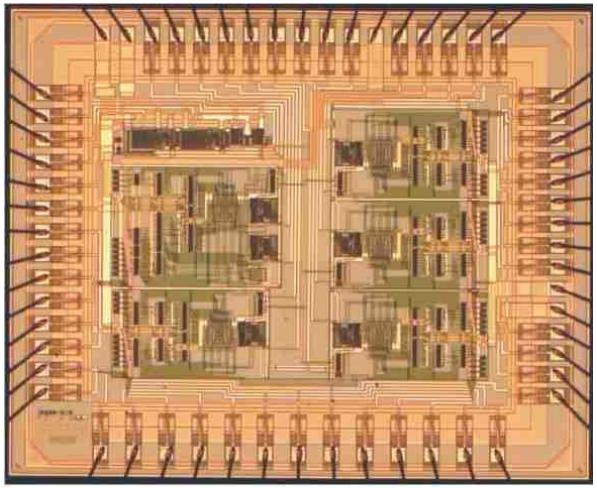
Outros CI´s Desenvolvidos



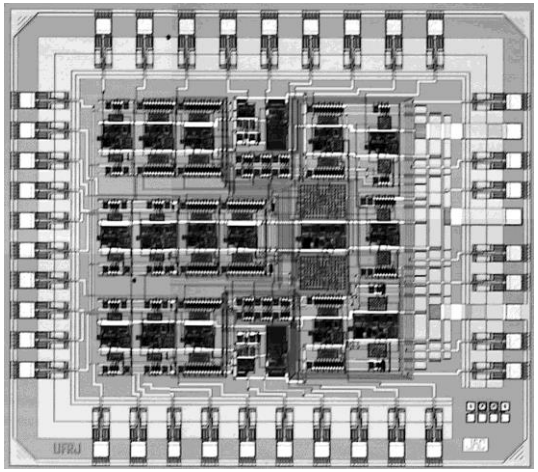
(a)



(b)

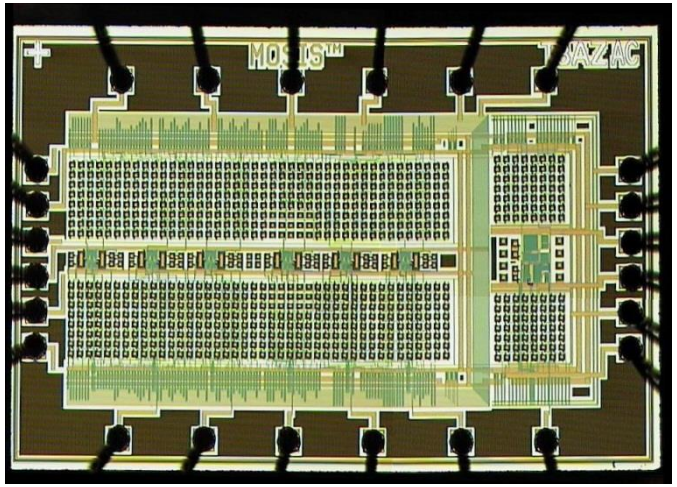


(c)

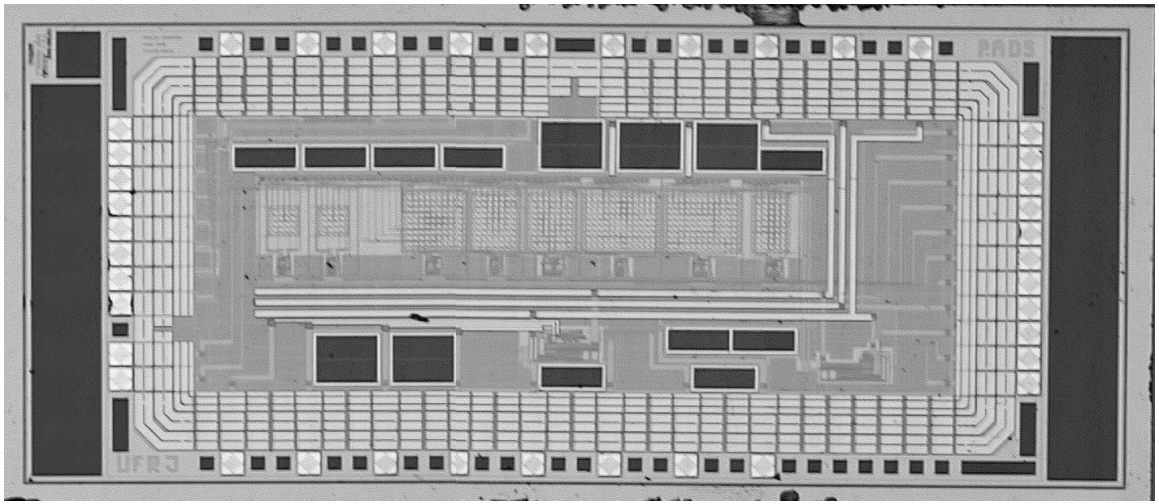


(d)

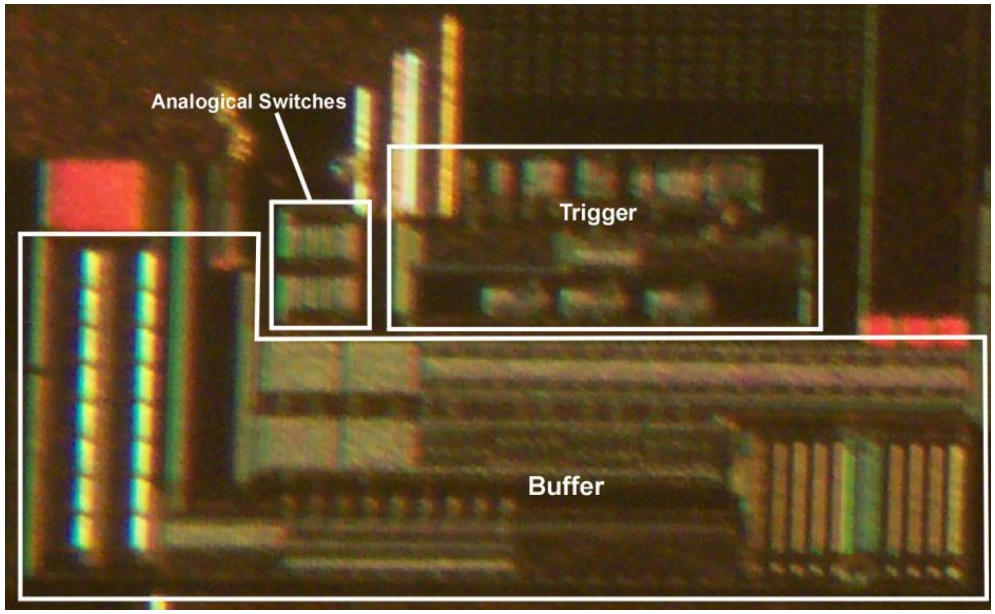
(a) Filtro decimador ; (b) filtro passa-baixas para vídeo; (c) filtro equalizador digitalmente programável ; (d) filtro decimador (0.8μm CMOS)



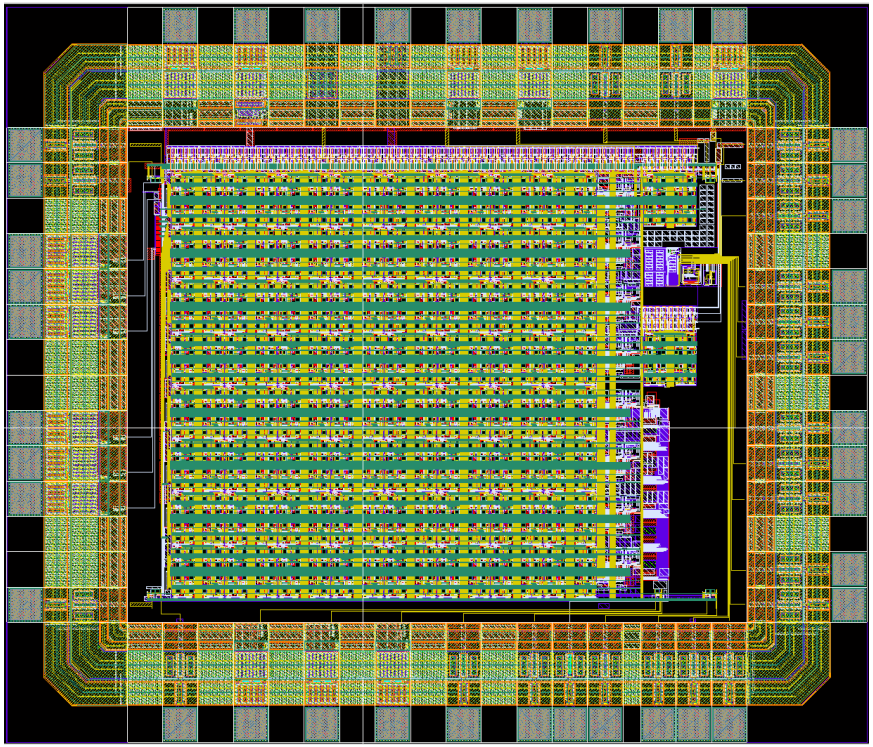
Filtro seletor de canais para interface Bluetooth de rádio (0.18 μm CMOS)



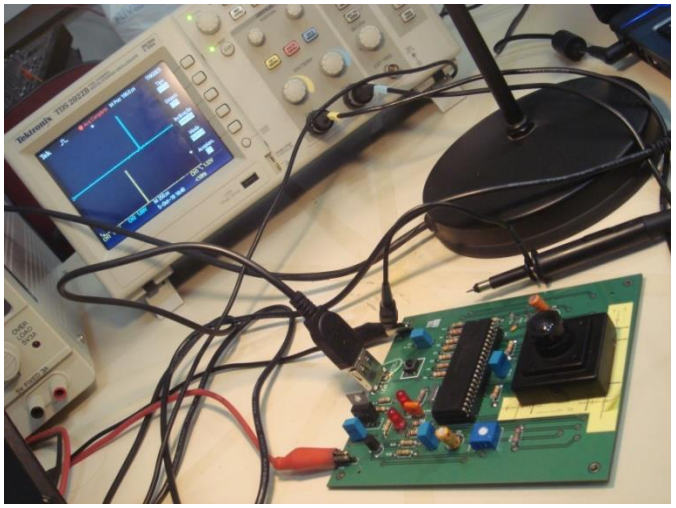
Filtro passa-banda – 20 kHz a 30 kHz (0.35 μm CMOS)



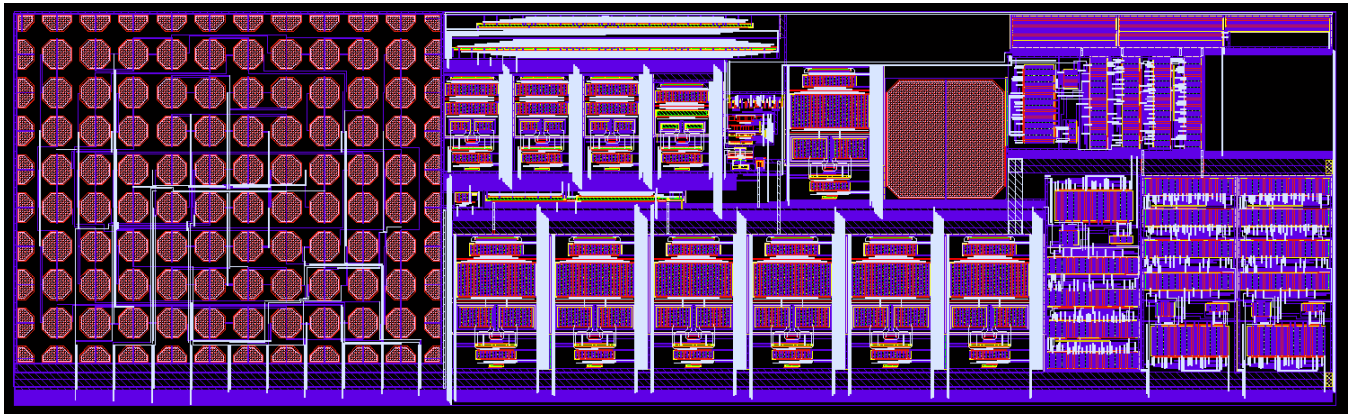
Demodulador AM monolítico (0.35 μm CMOS)



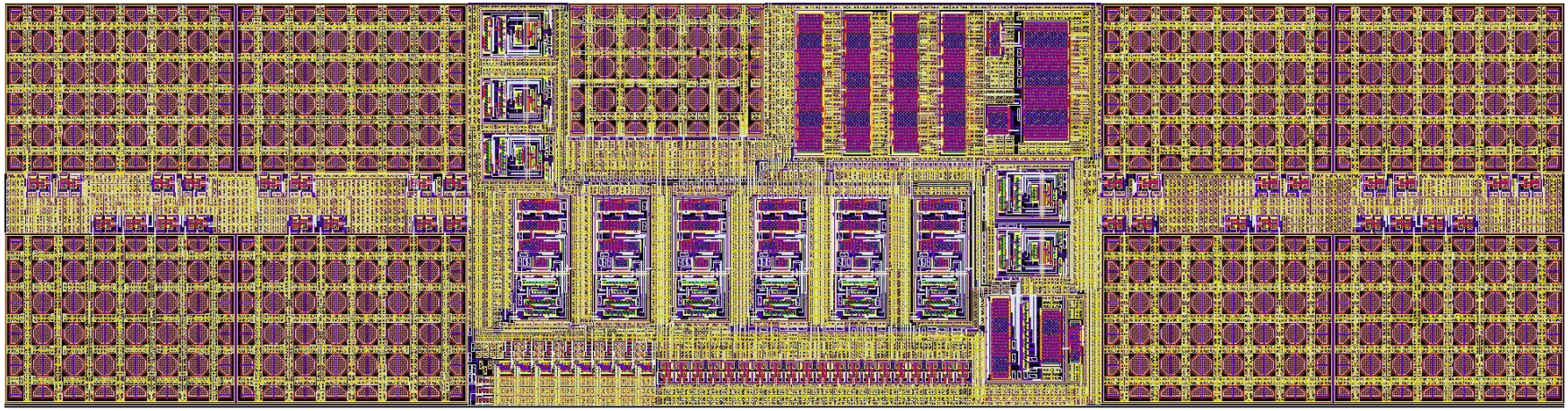
Compressão de dados no plano focal de câmeras digitais (0.35 μm CMOS)



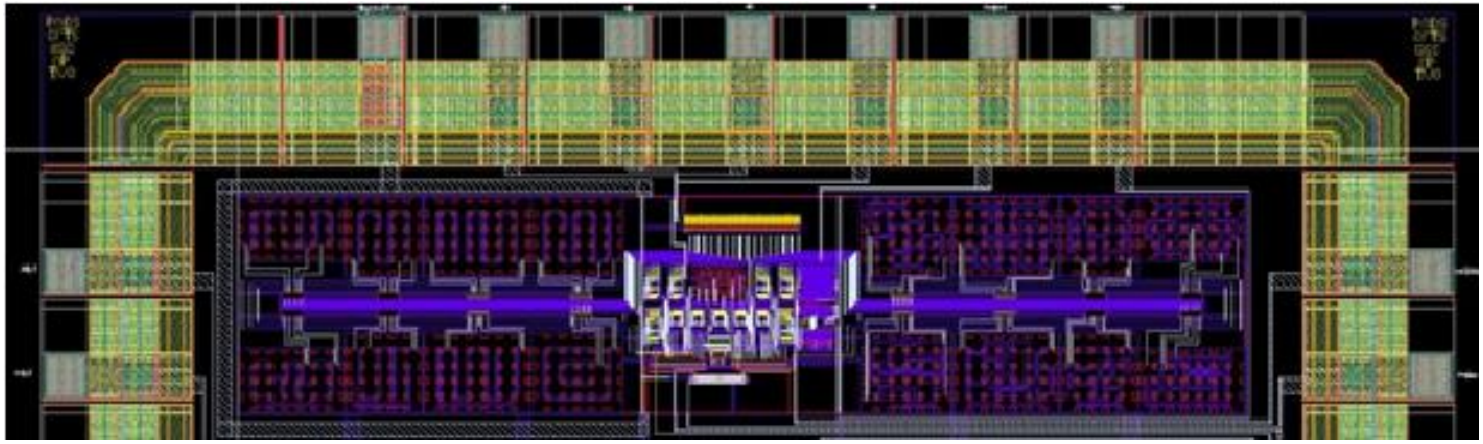
Placa de testes



PLL para sintonia automática de filtros *anti-aliasing* de baixas frequências GmC (0.35 μm CMOS)

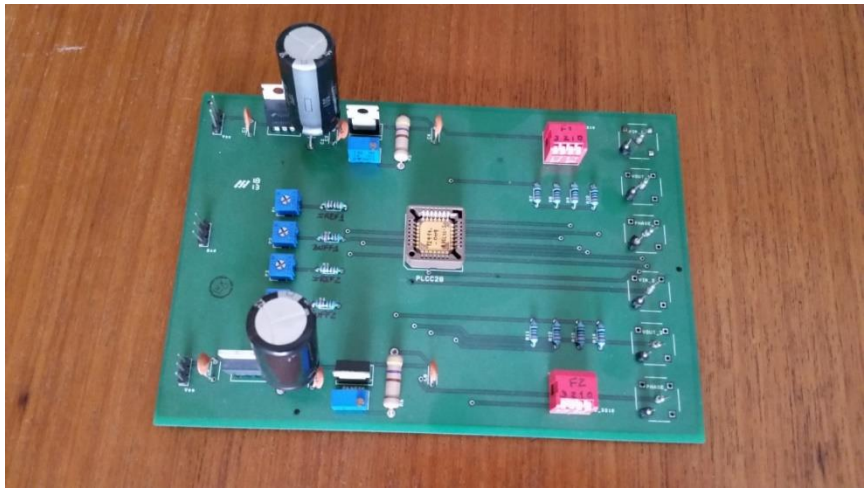


Circuito para a verificação experimental do casamento de capacitâncias (0.35 μm CMOS)



Circuito para a verificação experimental do casamento de capacitâncias – Versão 2 (0.35 μm CMOS)

Dimensões: 3.2 x 0.90 mm^2 ; Capacitância unitária: 100 fF



Placa de testes