Accurate On-Chip Capacitance Ratio Measurement Technique using a Switched-Capacitor Filter

Introduction

Applications in which capacitance matching is critical:

- Switched-capacitor filters, A/D, D/A and DC/DC converters.

Capacitance ratio error sources in CMOS ICs:

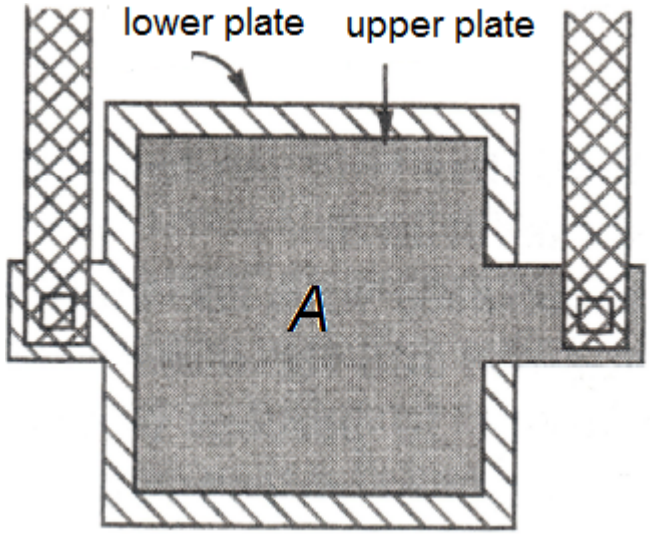
- Systematic errors;
- Process gradients (t_{ox});
- Mismatches.

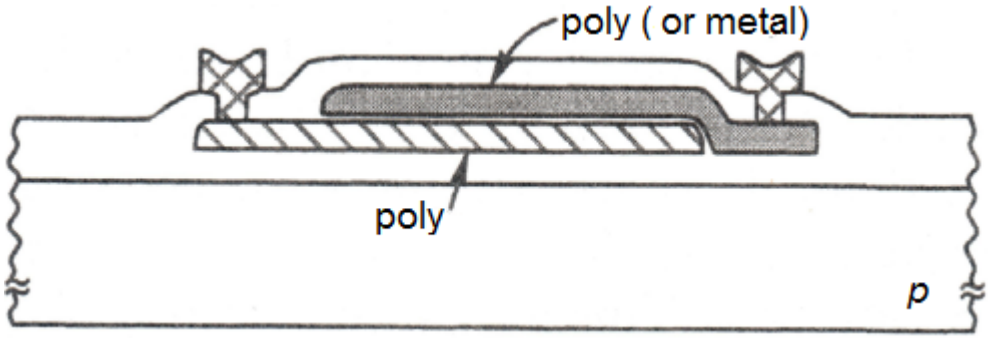
Techniques to improve capacitance ratio accuracy:

- Capacitors with the same area/perimeter ratio;
- Parallel connections of unit capacitors to realize each capacitance;
- Arrange unit capacitor arrays in common centroid geometry;
- Careful routing inside the capacitor array.

Capacitance Ratio
Error Sources

Capacitors in CMOS Technology





$C = AC_{ox}$

$C_{ox} = \varepsilon_{ox}/t_{ox}$

For 0.35 µm CMOS:

$\varepsilon_{ox} \approx 3.5 \times 10^{-13}$ F/cm

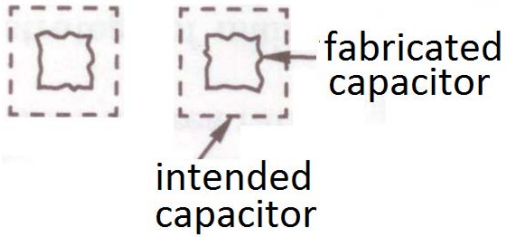
$t_{ox} \approx 10$ nm

$\Rightarrow C_{ox} \approx 3.5$ fF/µm^2

Capacitors in CMOS Technology

Capacitors too small:

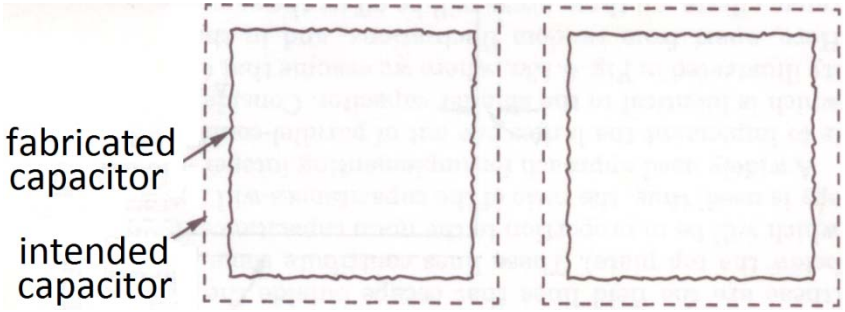
– The actual capacitance ratio can be significantly different from unity.



Larger capacitors:

– Better ratio accuracy;

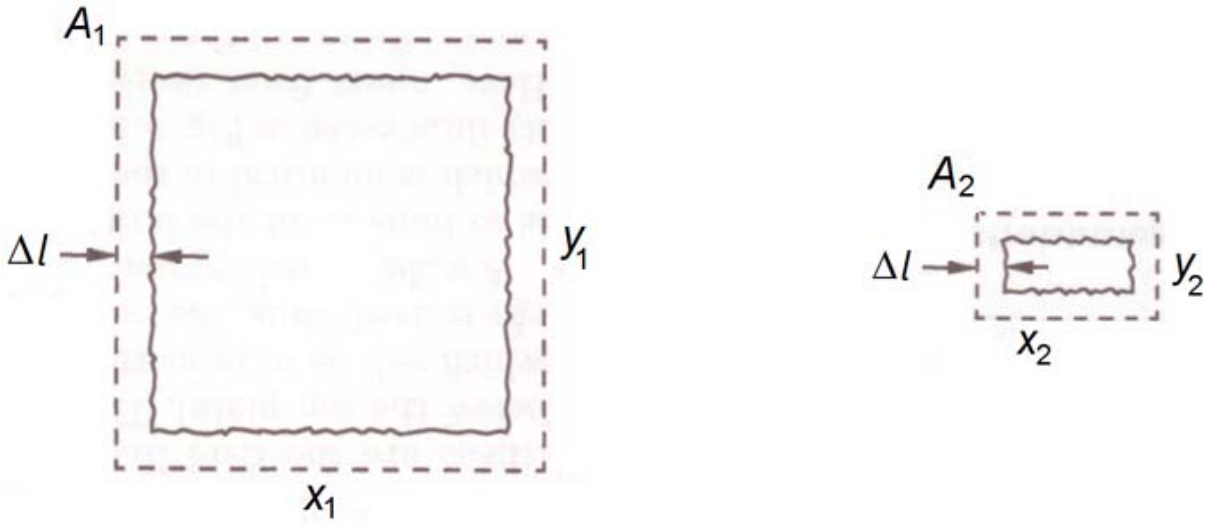
– However, if the plates are too large: (i) chip area may be excessive;
(ii) opposite regions of the two capacitors may be affected differently by the fabrication process (e.g., slight difference in oxide thickness);



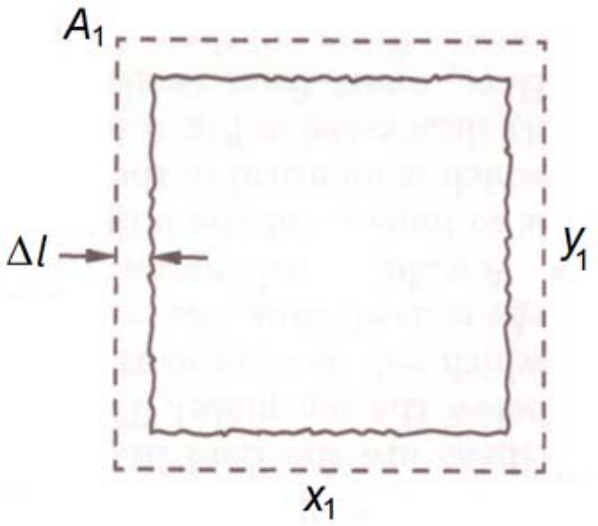
Capacitors in CMOS Technology

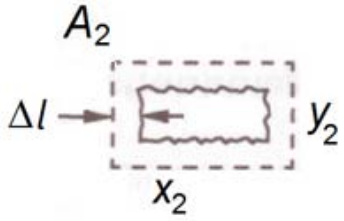
Sistematic errors:

- The relative area error of two capacitors will be the same if the nominal perimeter/area ratio is the same;
- Therefore the capacitance ratio will not be affected.



Capacitors in CMOS Technology





Let $A'_1 = (X_1 - 2\Delta l)(Y_1 - 2\Delta l)$

$$\approx X_1 Y_1 - 2\Delta l(X_1 + Y_1)$$

$$= A_1 - P_1 \Delta l$$

The relative area error is

$$\frac{\Delta A_1}{A_1} = -\frac{P_1 \Delta l}{A_1}$$

The capacitance ratio is

$$\frac{C'_1}{C'_2} = \frac{A'_1}{A'_2} = \frac{A_1\left(1 - \frac{P_1 \Delta l}{A_1}\right)}{A_2\left(1 - \frac{P_2 \Delta l}{A_2}\right)}$$

Therefore, if

$$\frac{P_1}{A_1} = \frac{P_2}{A_2}$$

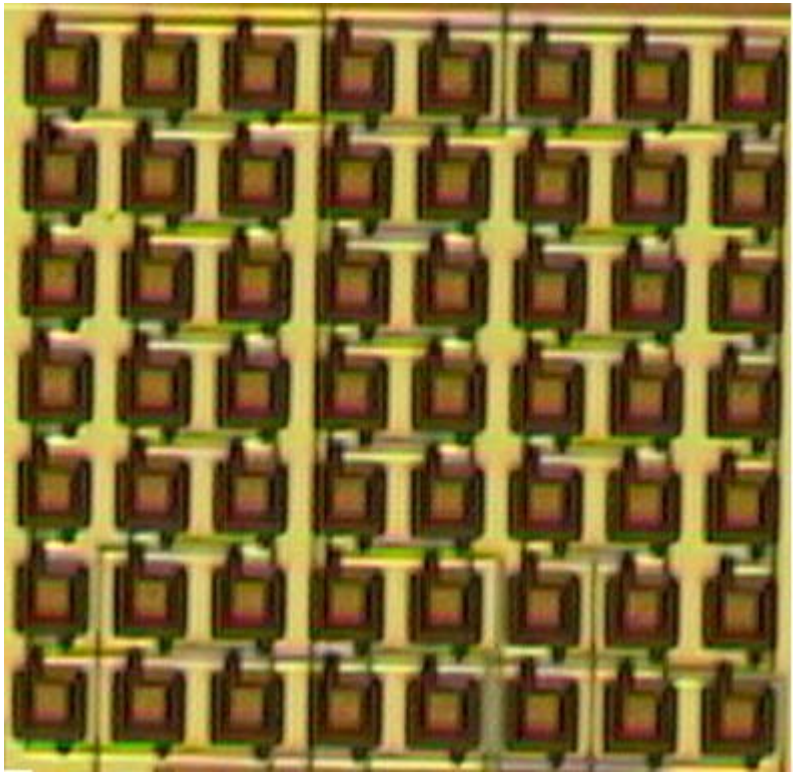
then

$$\frac{C'_1}{C'_2} = \frac{C_1}{C_2}$$

Capacitor Layout

Techniques to improve capacitance matching:

- Parallel connection of identical unit capacitors to implement each capacitance;
- Arrangement of unit capacitors in common centroid symmetry;
- Careful routing inside capacitor matrices.

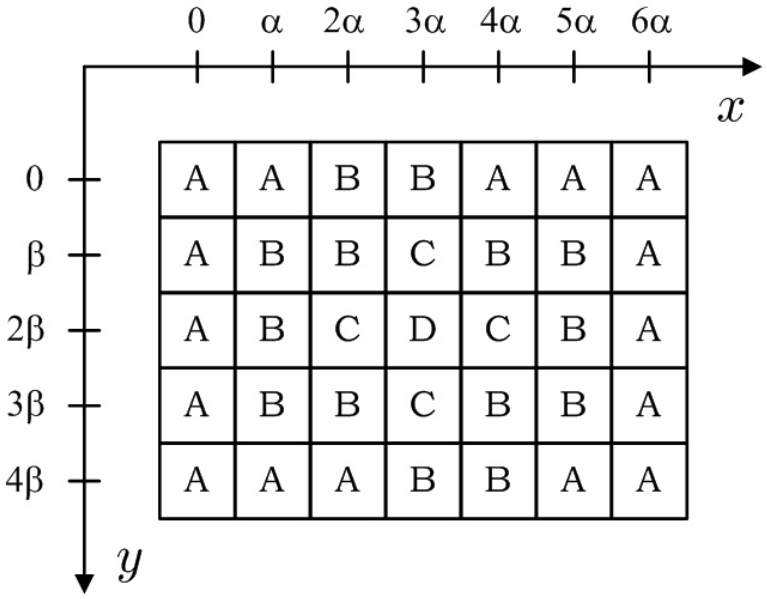


Unit capacitor: C = 100 fF

A = 5μm x 5μm

Capacitor Layout

Common centroid geometry - evaluation of the mean unit capacitance of each capacitor, assuming a linear model for t_{ox} variation:



$$\langle C_{xy} \rangle_A = \frac{1}{16} \cdot [16\,C + 48\,\alpha + 32\,\beta] = C + 3\,\alpha + 2\,\beta$$

$$\langle C_{xy} \rangle_B = \frac{1}{14} \cdot [14\,C + 42\,\alpha + 28\,\beta] = C + 3\,\alpha + 2\,\beta$$

$$\langle C_{xy} \rangle_C = \frac{1}{4} \cdot [4\,C + 12\,\alpha + 8\,\beta] = C + 3\,\alpha + 2\,\beta$$

$$\langle C_{xy} \rangle_D = C + 3\,\alpha + 2\,\beta$$

Capacitor Layout

Difficulties:

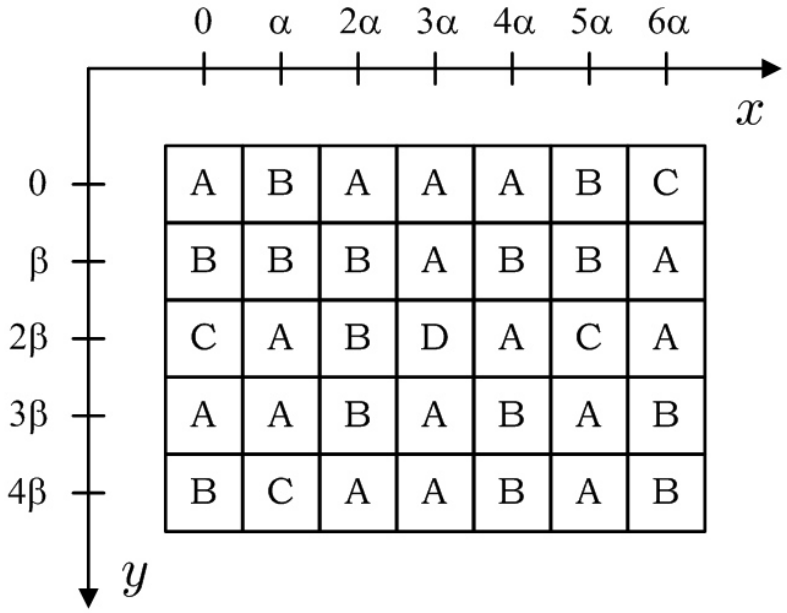
- Common centroid arrangement is not a simple task when the number of capacitance ratios is large;
- Common centroid geometry is not always possible;
- When it is possible, there are several alternatives;

Solutions:

- Develop an algorithm to search for the best arrangement among different possibilities;
- Find the optimal arrangement that doesn't have symmetry when common centroid is not possible.

Capacitor Layout

Example without common centroid, but insensitive to process gradient:



$$\langle C_{xy} \rangle_A = \frac{1}{16} \cdot [16\,C + 48\,\alpha + 32\,\beta] = C + 3\,\alpha + 2\,\beta$$

$$\langle C_{xy} \rangle_B = \frac{1}{14} \cdot [14\,C + 42\,\alpha + 28\,\beta] = C + 3\,\alpha + 2\,\beta$$

$$\langle C_{xy} \rangle_C = \frac{1}{4} \cdot [4\,C + 12\,\alpha + 8\,\beta] = C + 3\,\alpha + 2\,\beta$$

$$\langle C_{xy} \rangle_D = C + 3\,\alpha + 2\,\beta$$

The Allpass Filter

The Allpass Filter

A transfer function $A(z)$ whose frequency response magnitude is constant, for example,

$$\left|A\left(e^{j\omega}\right)\right| = 1, \qquad \text{for all } \omega$$

is called an *allpass transfer function*.

A circuit or system that has this property is an allpass “filter”.

The Allpass Filter

N^{th}-order allpass transfer function:

$$A(z) = \frac{a_N + a_{N-1}z^{-1} + \ldots + a_1 z^{-N+1} + z^{-N}}{1 + a_1 z^{-1} + \ldots + a_{N-1}z^{-N+1} + a_N z^{-N}}$$

Can be expressed in the general form

$$A(z) = \frac{z^{-N} D(z^{-1})}{D(z)}$$

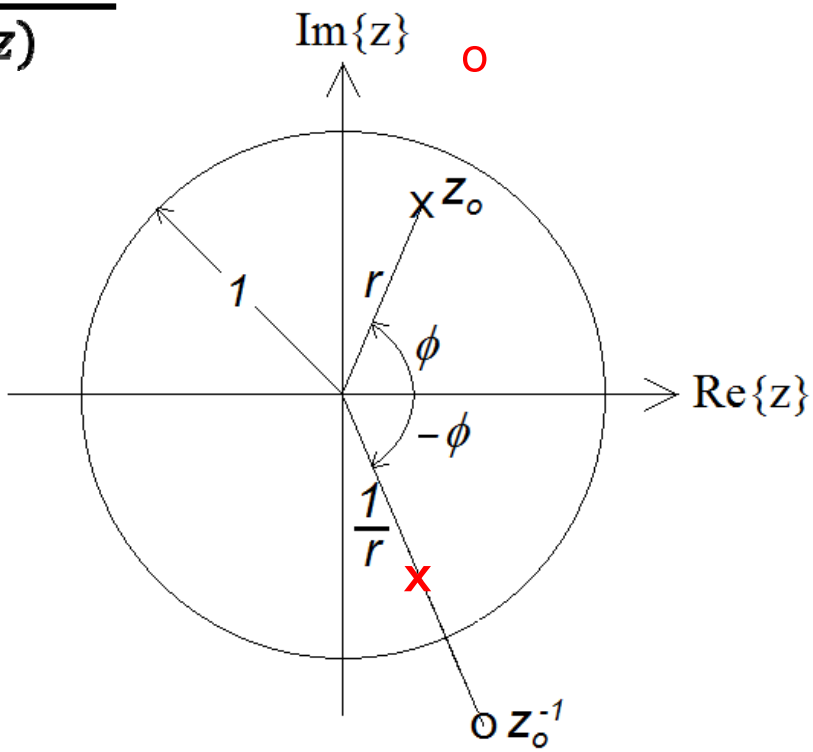
(i) If $z_o = re^{j\phi}$ is a pole of $A(z)$:

⇛ $z_o^{-1} = (1/r)e^{-j\phi}$ is a zero of $A(z)$

(ii) If the coefficients of $A(z)$ are real:

⇛ $(z_o)^* = re^{-j\phi}$ is a pole of $A(z)$

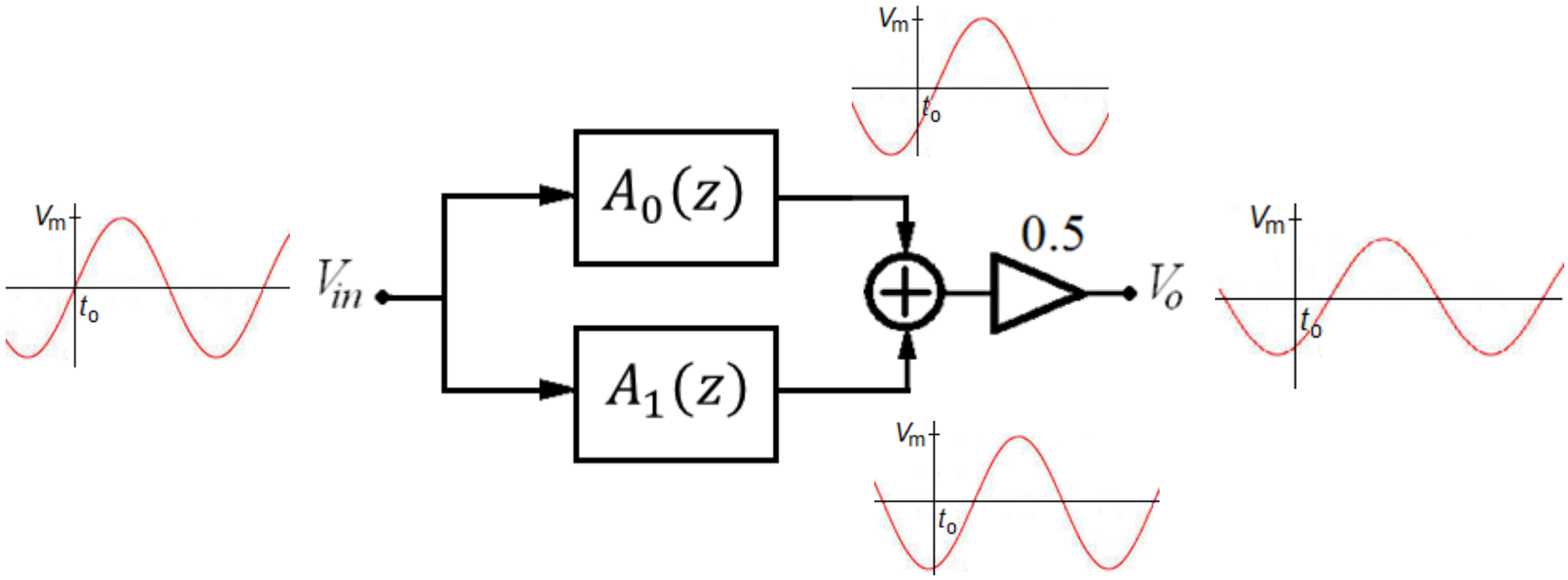
⇛ $(z_o^{-1})^* = (1/r)e^{j\phi}$ is a zero of $A(z)$



The Allpass Filter

Classical transfer functions (Butterworth, Chebyshev and elliptic) of odd degree can be decomposed as:

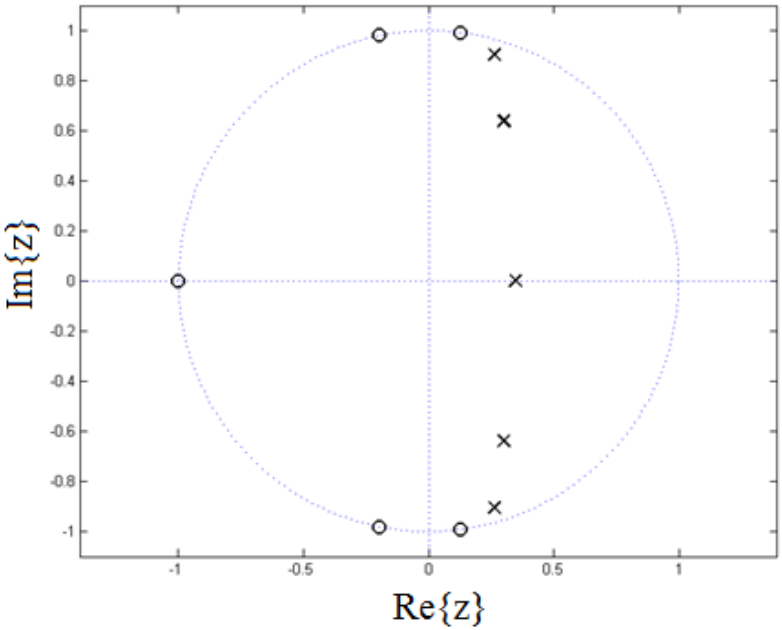
$$H(z) = \frac{1}{2}\{A_0(z) + A_1(z)\}$$

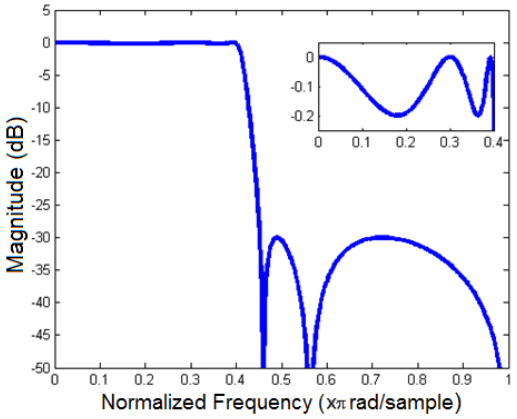


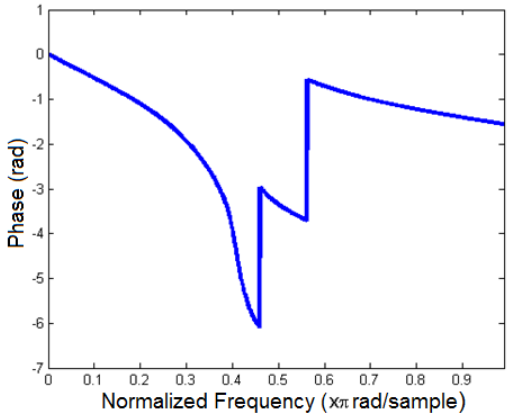
Decomposition in Allpass Sections

Ex.: 5th order elliptic lowpass filter:

$f_s = 18\ kHz;\ f_p = 3.6\ kHz;\ f_r = 4.5\ MHz;\ r_p \leq 0.2\ dB;\ A_r \geq 30\ dB.$

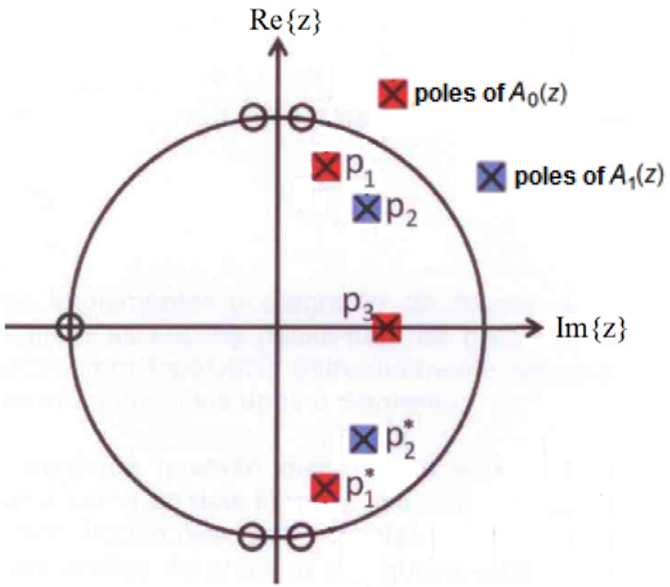


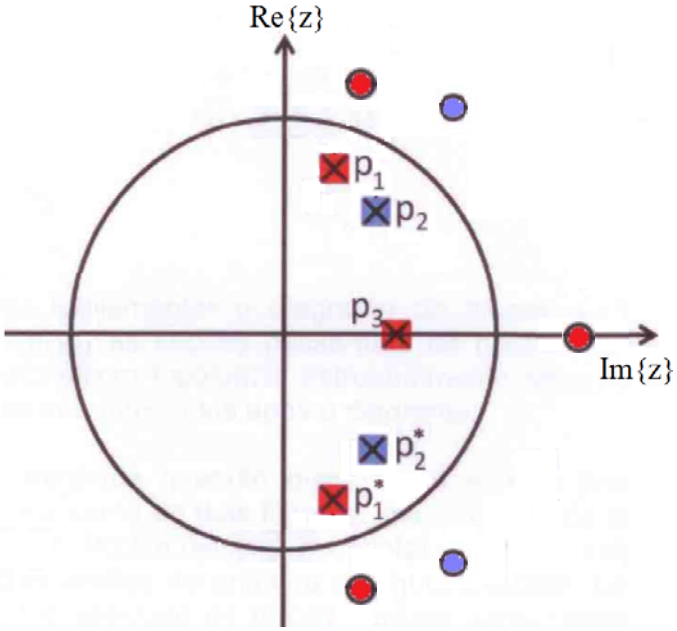




Decomposition in Allpass Sections

Pole interlacing property: a simple approach to identify the poles of $A_0(z)$ and $A_1(z)$:





5th order elliptic lowpass filter

$f_s = 18\text{kHz};\ f_p = 3.6\text{kHz};\ f_r = 4.5\text{kHz};$

$r_p \le 0.2$ dB; $A_r \ge 30$ dB.

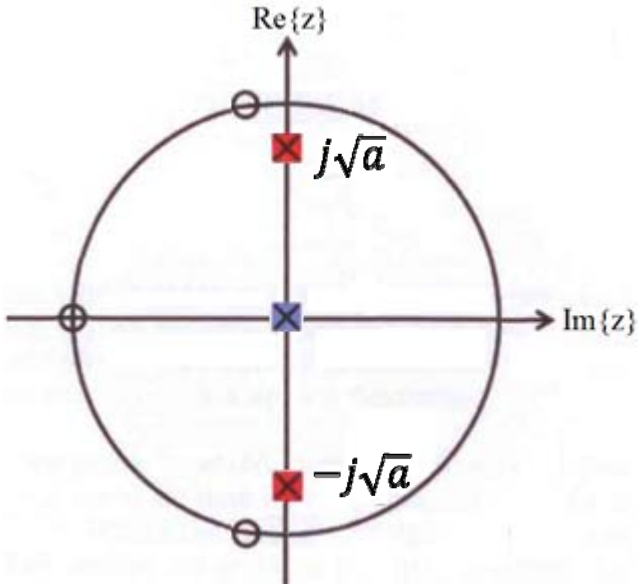
$$A_o(z) = \frac{-0.308+1.068z^{-1}-0.872z^{-2}+z^{-3}}{1-0.872z^{-1}+1.0682z^{-2}-0.308z^{-3}}$$

$$A_1(z) = \frac{0.499-0.600z^{-1}+z^{-2}}{1-0.600z^{-1}+0.499z^{-2}}$$

Capacitance Ratio Measurement Technique

Capacitance Ratio Measurement Technique

Let us consider a 3rd order lowpass elliptic filter, whose poles are on the imaginary axis:



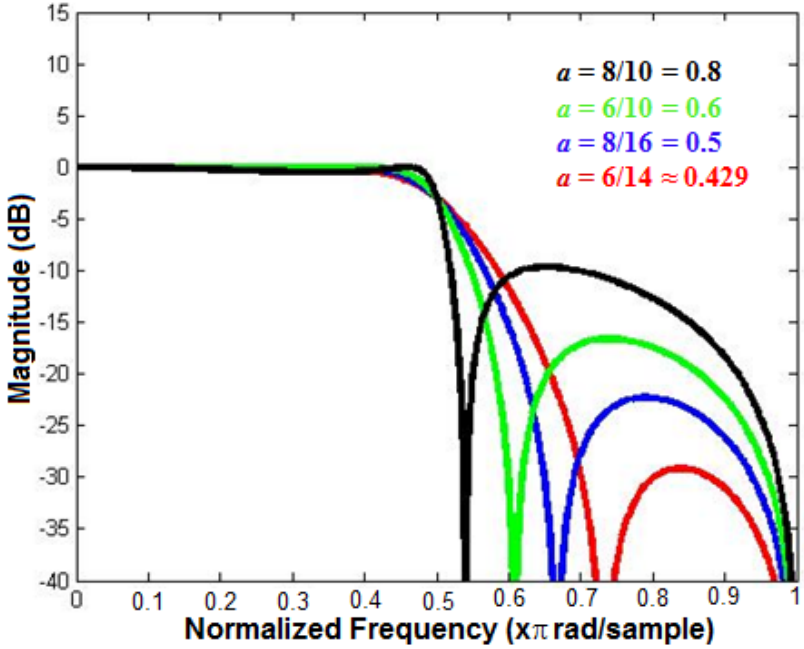
In this case:

$$A_o(z) = \frac{a + z^{-2}}{1 + az^{-2}}\ ; \quad A_1(z) = z^{-1} \quad \Rightarrow \quad H(z) = \frac{1}{2}\left(\frac{a + z^{-2}}{1 + az^{-2}} + z^{-1}\right)$$

Capacitance Ratio Measurement Technique

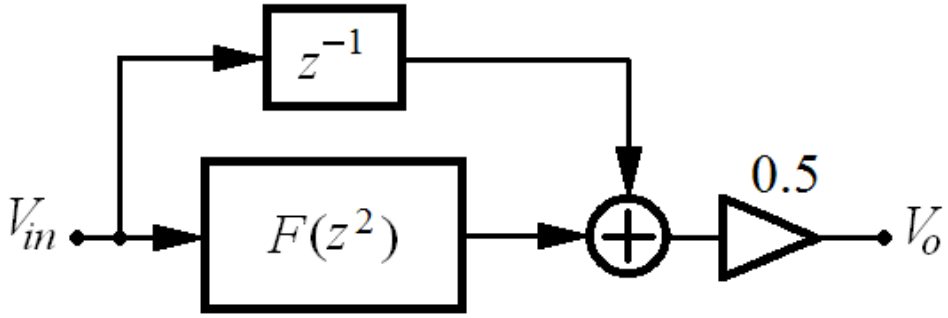
The magnitude frequency response is zero at the angular frequency

$$\omega_n = \cos^{-1}\left(\frac{a-1}{2a}\right)$$



Capacitance Ratio Measurement Technique

Realization of *H*(z):

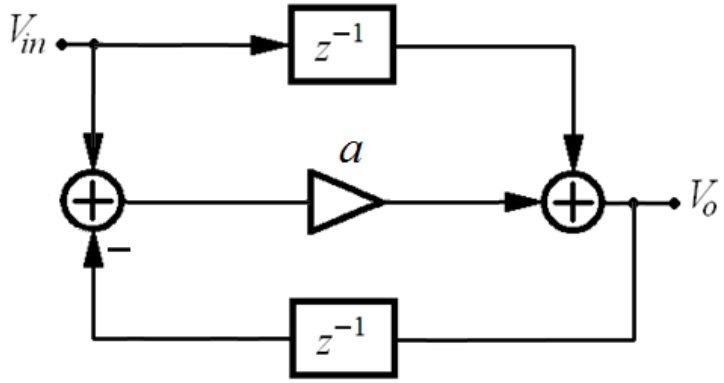


F(*z*) is the 1st order allpass filter

$$F(z) = \frac{z^{-1} + a}{1 + az^{-1}}$$

Capacitance Ratio Measurement Technique

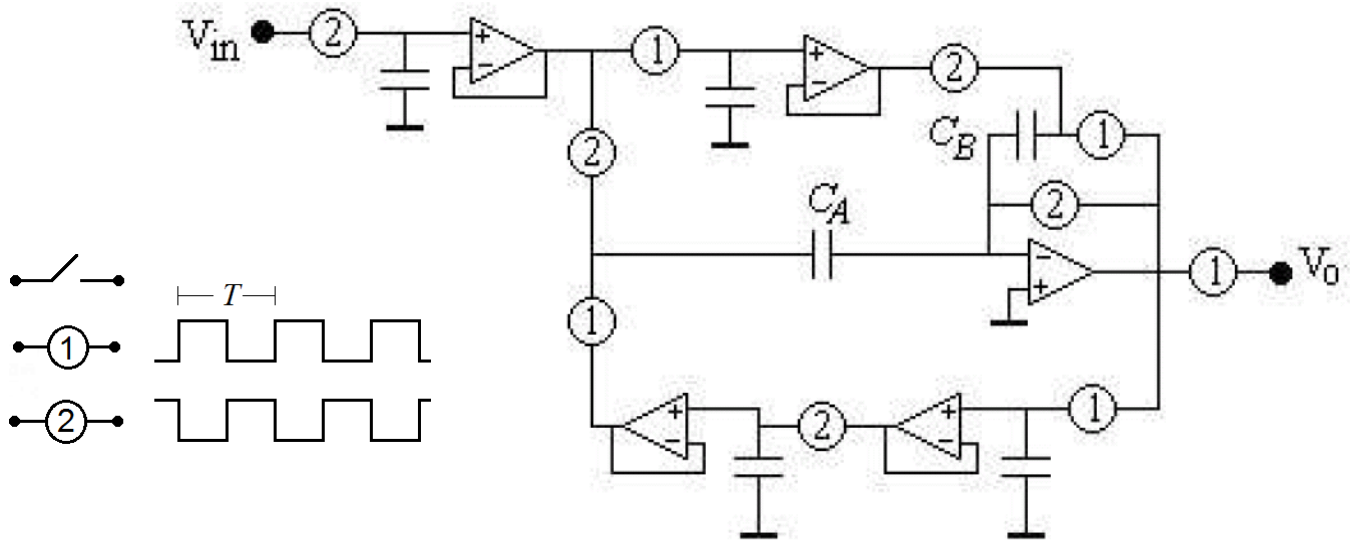
Realization of *F*(*z*) by a *structurally* allpass filter:



$$F(z) = \frac{z^{-1} + a}{1 + az^{-1}}$$

Capacitance Ratio Measurement Technique

Realization of $F(z)$ by a structurally allpass switched-capacitor filter:

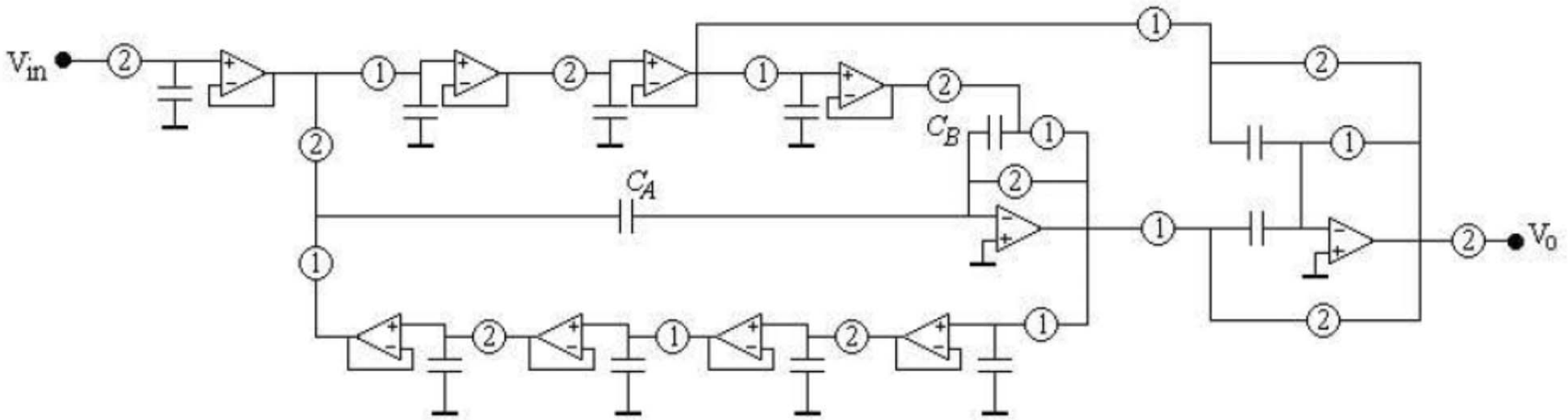


$$F(z) = z^{-1/2}\frac{z^{-1} + C_A/C_B}{1 + (C_A/C_B)z^{-1}}$$

$\alpha = C_A/C_B$ is the capacitance ratio of interest.

Capacitance Ratio Measurement Technique

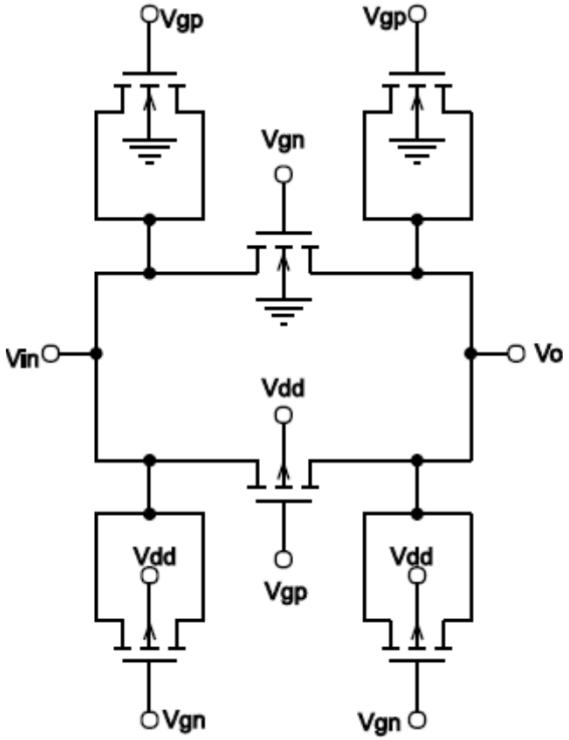
Realization of $F(z^2)$ and the adder:



$$H(z) = \frac{1}{2}\left(\frac{a + z^{-2}}{1 + az^{-2}} + z^{-1}\right)$$

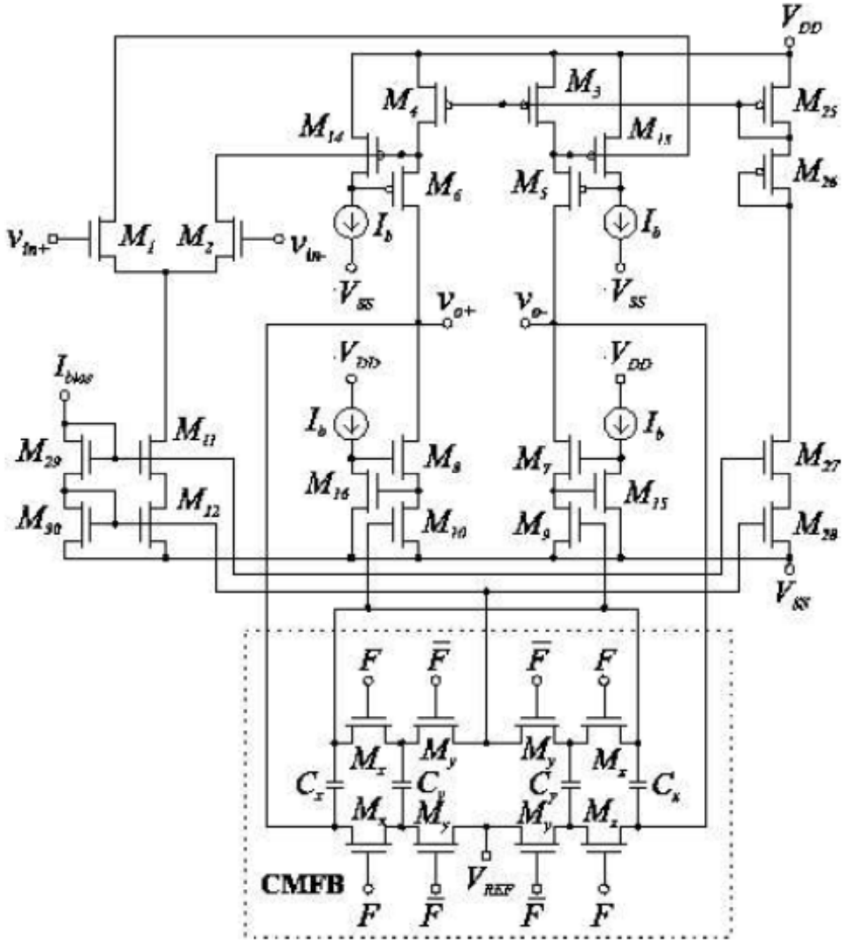
Analog Switches

Both complementary and dummy devices were employed to reduce charge injection and clock leakage:



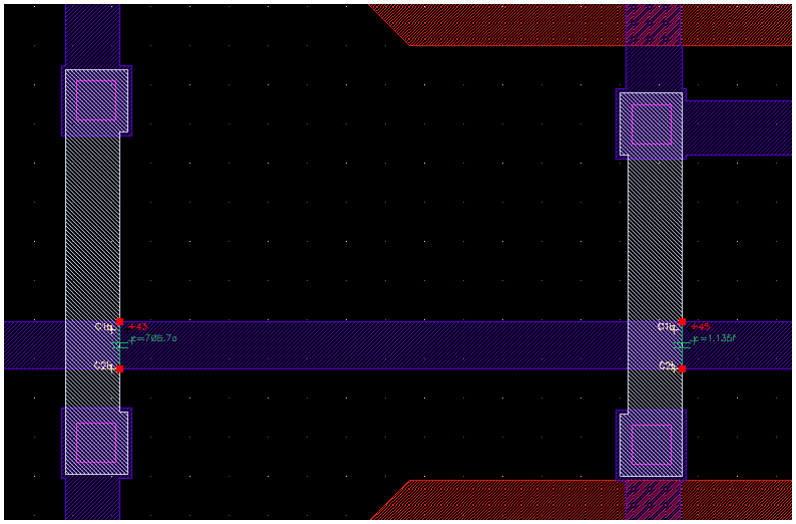
Amplifiers

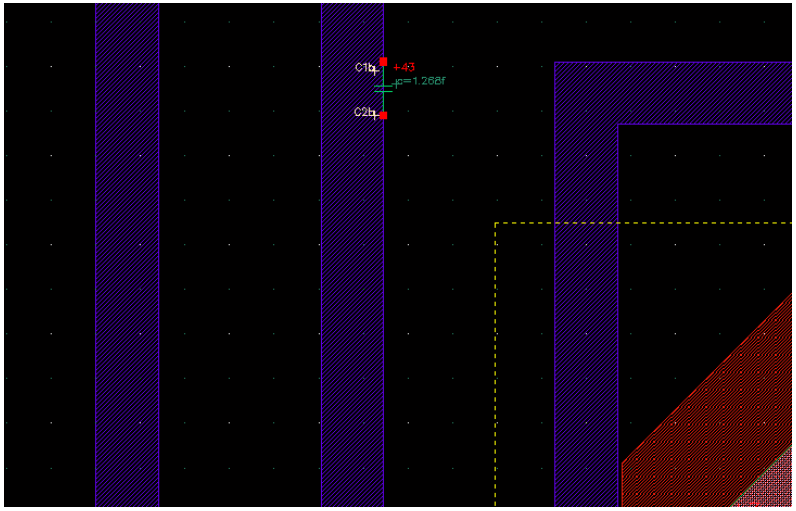
Fully differential folded cascode amplifier with gain boosting:



Layout

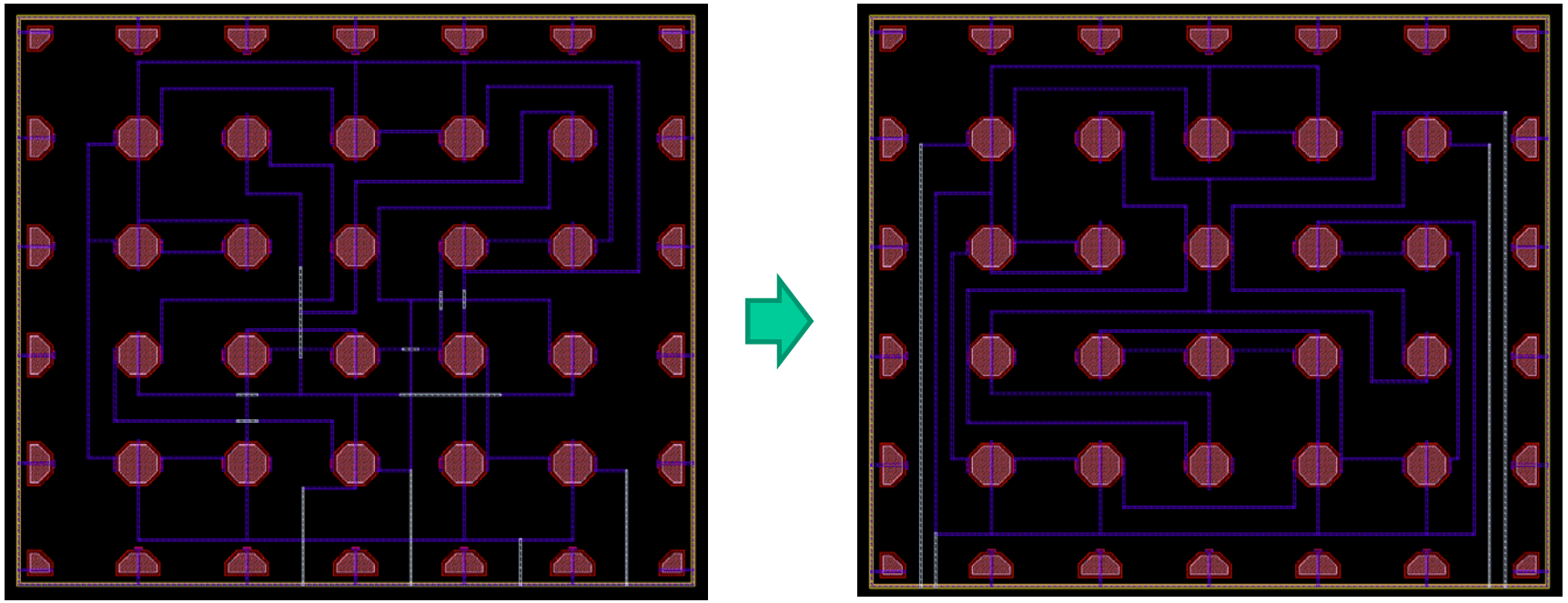
crossover capacitances



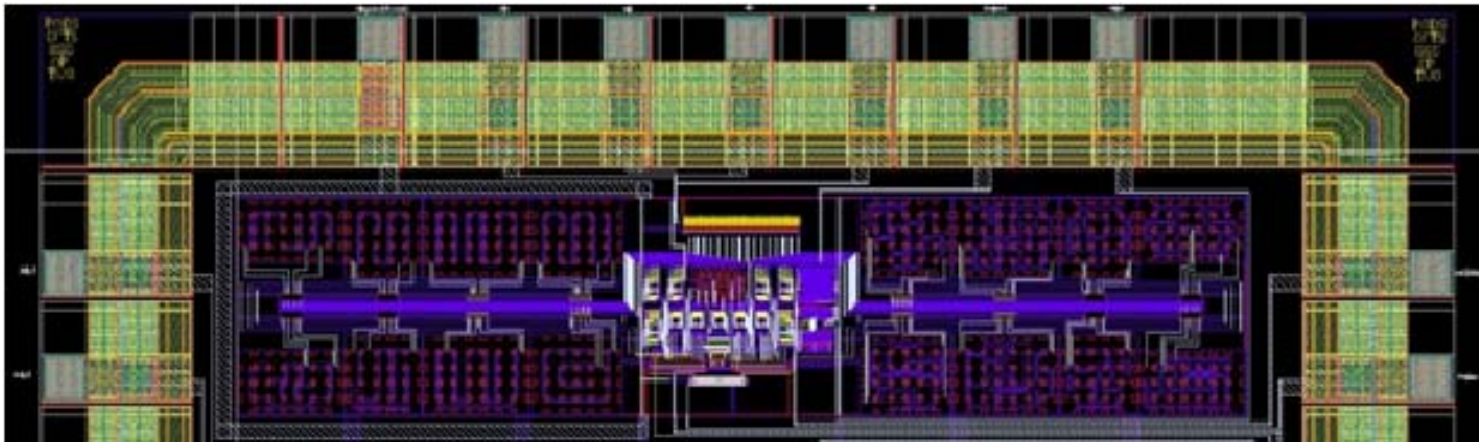


crosstalk capacitances

Layout

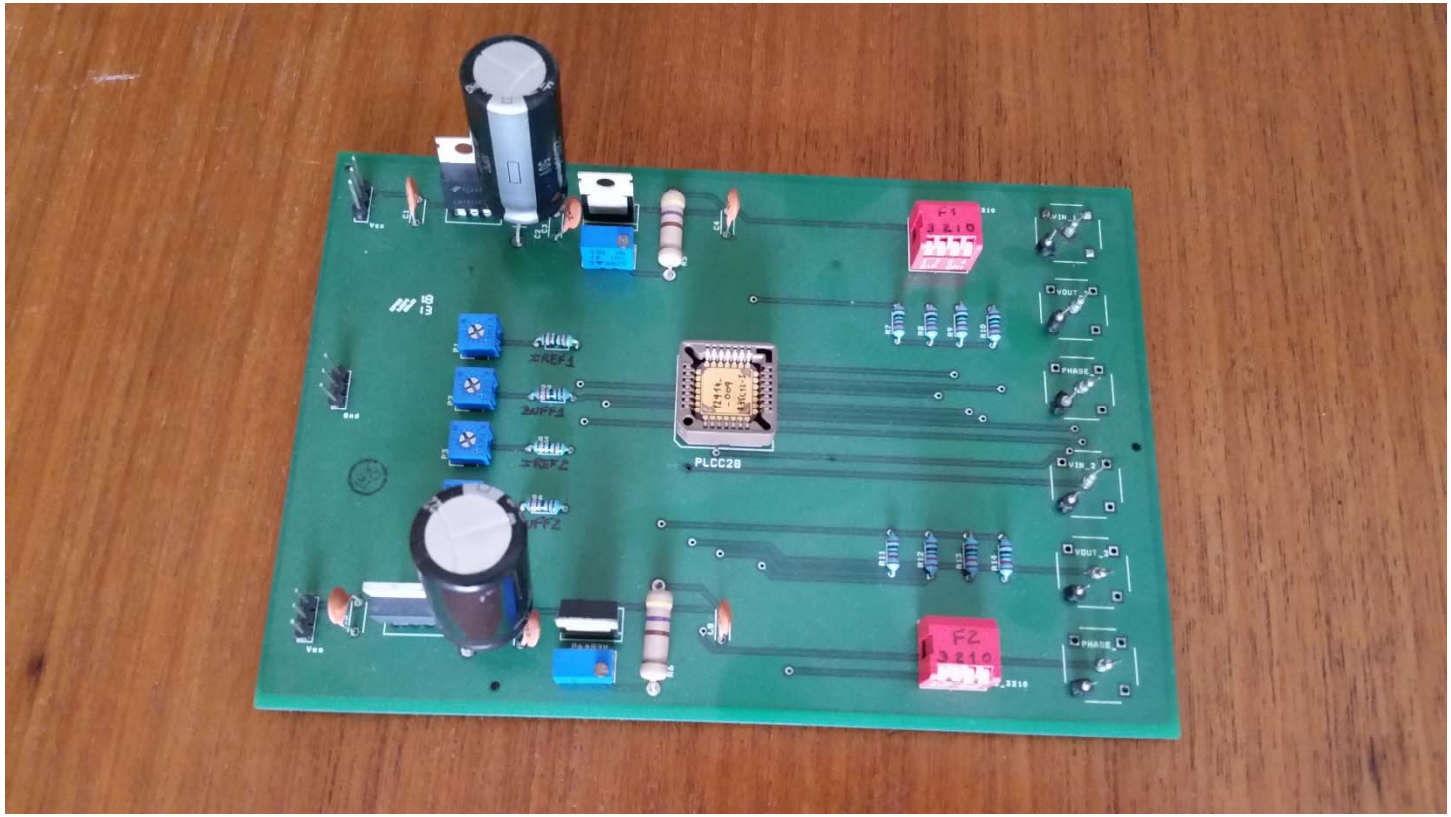


Experimental Results



Process technology: 0.35 μm CMOS
Dimensions: 3.2 x 0.90 mm^2
Unit capacitance: 100 fF

Experimental Results



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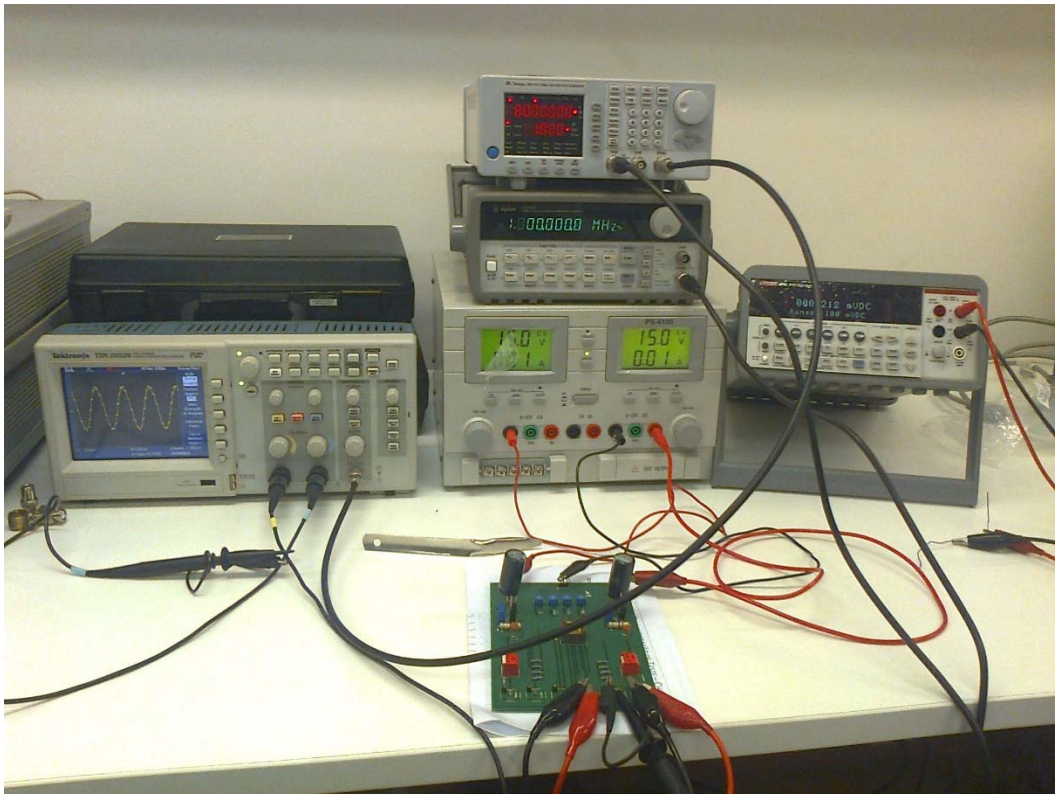

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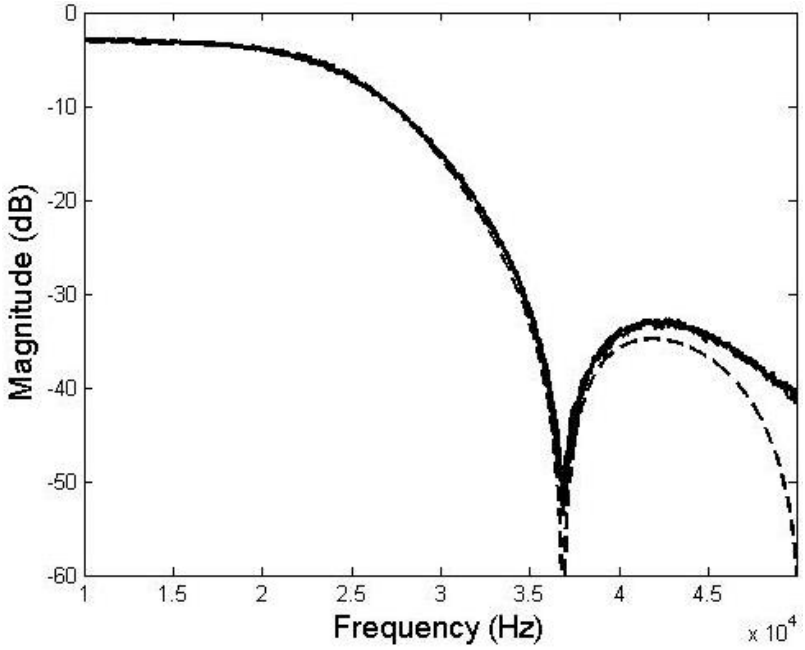

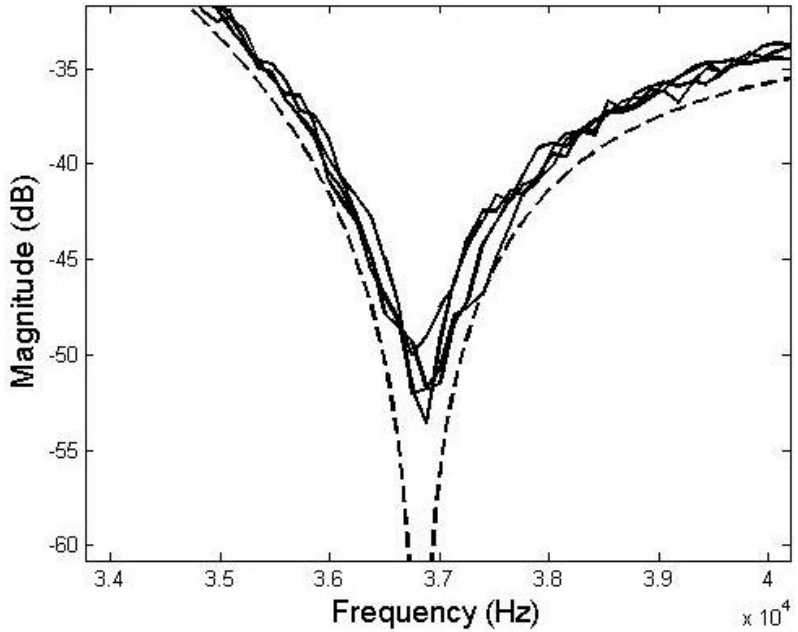

C_A = 600 fF; C_B= 1.4 pF

Nominal sampling frequency (f_s): 100 kHz

Measured sampling frequency = 100.576 kHz

Theoretical zero frequency = 36.834 kHz

Measured zero frequencies = 36.752 kHz and 36.880 kHz

Ideal capacitance ratio = 3/7 = 0.429

Measured capacitance ratios = 0.4279, 0.4281, 0.4292, 0.4294

Mean error = - 0.082%