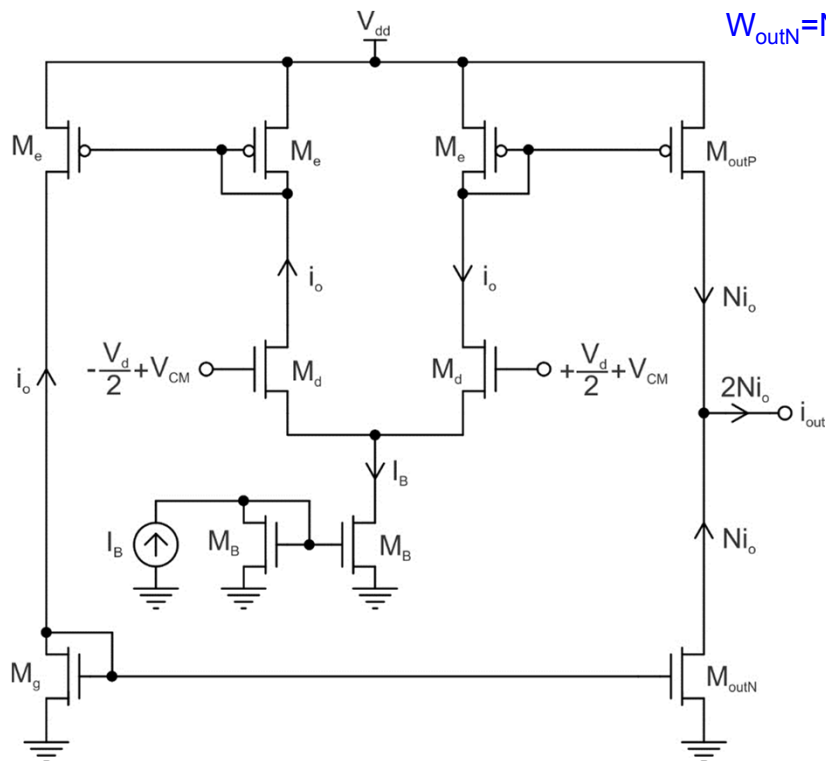


Amplificador Operacional de Transcondutância - OTA

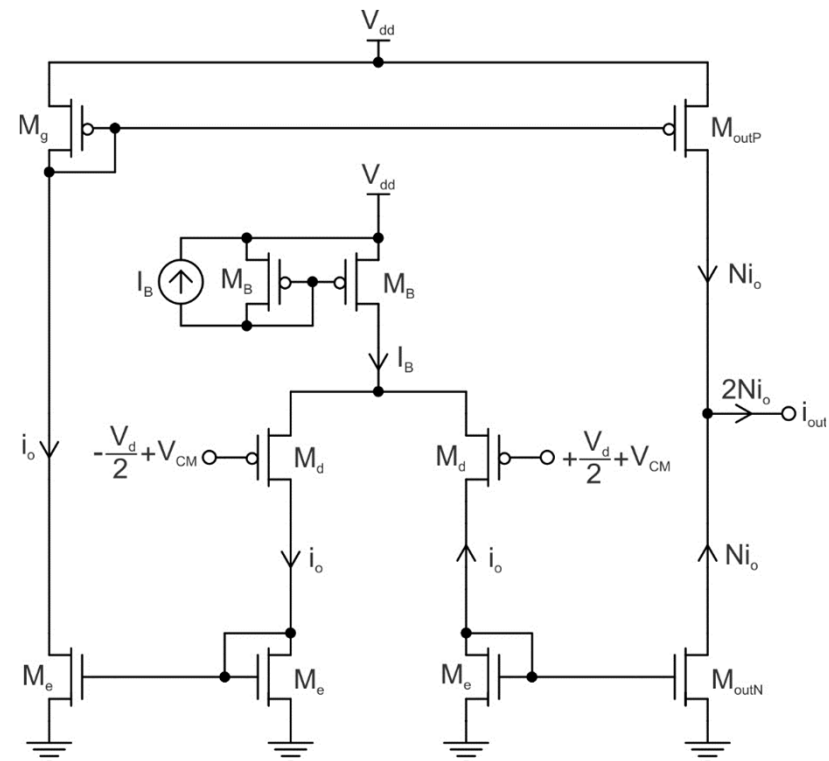
Amplificadores Operacionais de Transcondutância (OTA) são dispositivos muito usados na microeletrônica, principalmente no projeto de filtros a capacitores chaveados (SC) e filtros contínuos no tempo (gm-C). Sua impedância de saída é muito elevada, e a corrente de saída é proporcional ao ganho de transcondutância g_{m_d} do amplificador diferencial de entrada. Quando usado com carga capacitiva, torna-se um integrador. Os polos produzidos pelas capacitâncias parasitas estão em frequências altas, de forma que o capacitor de saída define o polo dominante, dispensando compensação em frequência na maioria das aplicações.

Versão single-ended - NMOS



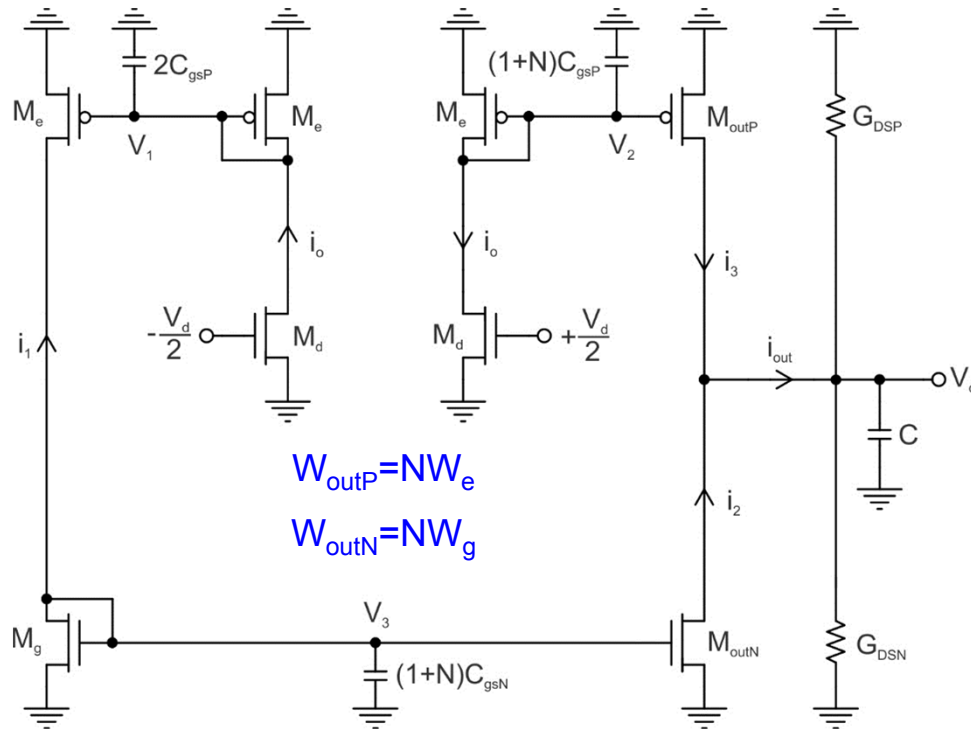
$$W_{outP} = NW_e$$
$$W_{outN} = NW_g$$

Versão single-ended - PMOS



Análise AC de Pequenos Sinais com Carga Capacitiva

Versão single-ended - NMOS



$$I_{out} = I_2 + I_3$$

$$I_0 = gm_d \frac{V_d}{2} \rightarrow V_1 = \frac{\frac{I_0}{gm_e}}{s \frac{2C_{gsP}}{gm_e} + 1}$$

$$I_1 = gm_e V_1 \rightarrow V_3 = \frac{-\frac{I_1}{gm_g}}{s \frac{(1+N)C_{gsN}}{gm_g} + 1}$$

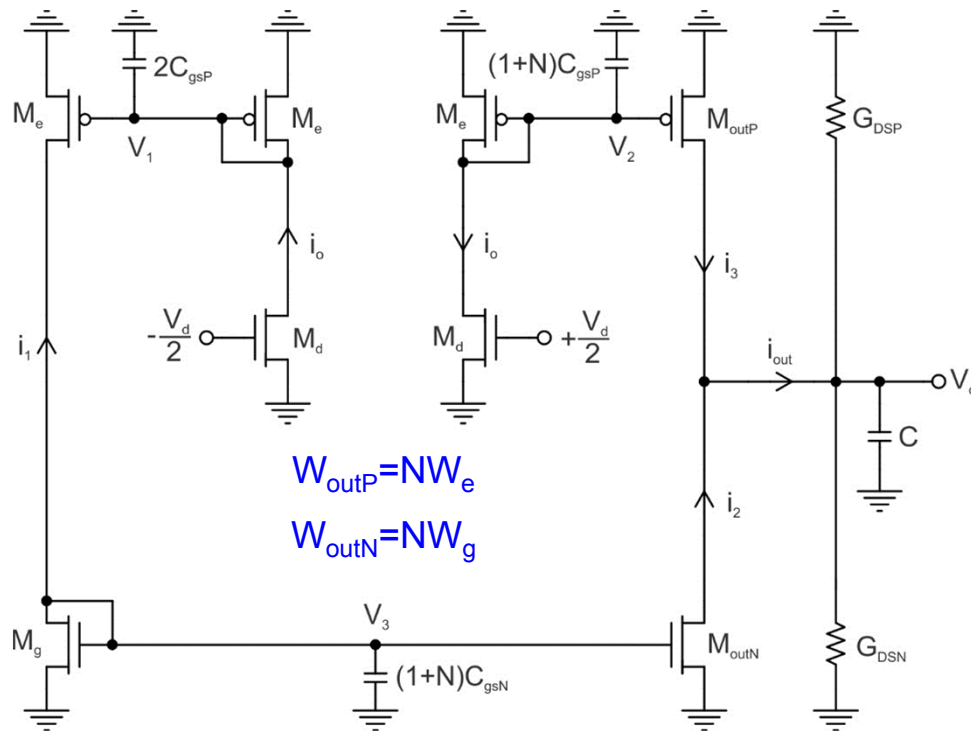
$$V_3 = \frac{-\frac{gm_e}{gm_g} V_1}{s \frac{(1+N)C_{gsN}}{gm_g} + 1} \rightarrow I_2 = -N gm_g V_3$$

$$V_2 = \frac{-\frac{I_0}{gm_e}}{s \frac{(1+N)C_{gsP}}{gm_e} + 1} \rightarrow I_3 = -N gm_e V_2$$

$$\frac{I_{out}}{V_d} = \frac{\left(s \frac{(1+N)C_{gsP}}{gm_e} + 1 \right) + \left(s \frac{2C_{gsP}}{gm_e} + 1 \right) \left(s \frac{(1+N)C_{gsN}}{gm_g} + 1 \right) N gm_d}{\left(s \frac{2C_{gsP}}{gm_e} + 1 \right) \left(s \frac{(1+N)C_{gsN}}{gm_g} + 1 \right) \left(s \frac{(1+N)C_{gsP}}{gm_e} + 1 \right) 2}$$

Análise AC de Pequenos Sinais com Carga Capacitiva

Versão single-ended - NMOS



$$I_{out} = I_2 + I_3$$

$$I_0 = gm_d \frac{V_d}{2} \quad \longrightarrow \quad V_1 = \frac{\frac{I_0}{gm_e}}{s \frac{2C_{gs_p}}{gm_e} + 1}$$

$$I_1 = gm_e V_1 \xrightarrow{\text{red}} V_3 = \frac{-\frac{I_1}{gm_g}}{s \frac{(1+N)C_{gs_N}}{gm_g} + 1}$$

$$V_3 = \frac{-\frac{gm_e}{gm_g} V_1}{(1+N)C_{gs_N} + 1} \rightarrow I_2 = -N gm_g V_3$$

$$V_2 = \frac{-\frac{I_0}{gm_e}}{s\frac{(1+N)C_{gs_p}}{gm_e} + 1} \rightarrow I_3 = -Ngm_e V_2$$

$$\frac{I_{out}}{V_d} = \frac{\left(s \frac{(1+N)C_{gs_P}}{gm_e} + 1 \right) + \left(s \frac{2C_{gs_P}}{gm_e} + 1 \right) \left(s \frac{(1+N)C_{gs_N}}{gm_g} + 1 \right)}{\left(s \frac{2C_{gs_P}}{gm_e} + 1 \right) \left(s \frac{(1+N)C_{gs_N}}{gm_g} + 1 \right) \left(s \frac{(1+N)C_{gs_P}}{gm_e} + 1 \right)} \frac{Ngm_d}{2}$$

$$\frac{I_{out}}{V_d} = \frac{\left(s \frac{(1+N)C_{gs_P}}{gm_e} + 1 \right) + \left(s \frac{2C_{gs_P}}{gm_e} + 1 \right) \left(s \frac{(1+N)C_{gs_N}}{gm_g} + 1 \right)}{\left(s \frac{2C_{gs_P}}{gm_e} + 1 \right) \left(s \frac{(1+N)C_{gs_N}}{gm_g} + 1 \right) \left(s \frac{(1+N)C_{gs_P}}{gm_e} + 1 \right)} \frac{Ngm_d}{2} \rightarrow V_0 = \frac{\frac{I_{out}}{(G_{DS_P} + G_{DS_N})}}{\left(s \frac{C}{G_{DS_P} + G_{DS_N}} + 1 \right)}$$

↓ N=1

$$\frac{I_{out}}{V_d} = \frac{gm_d \left(s \frac{C_{gs_N}}{gm_g} + 1 \right)}{\left(s \frac{2C_{gs_P}}{gm_e} + 1 \right) \left(s \frac{2C_{gs_N}}{gm_g} + 1 \right)}$$

$$\begin{matrix} gm_e \gg G_{DS_P} + G_{DS_N} \\ gm_g \gg G_{DS_P} + G_{DS_N} \end{matrix} \rightarrow V_0 = \frac{\frac{gm_d}{(G_{DS_P} + G_{DS_N})}}{\left(s \frac{C}{G_{DS_P} + G_{DS_N}} + 1 \right)} V_d$$

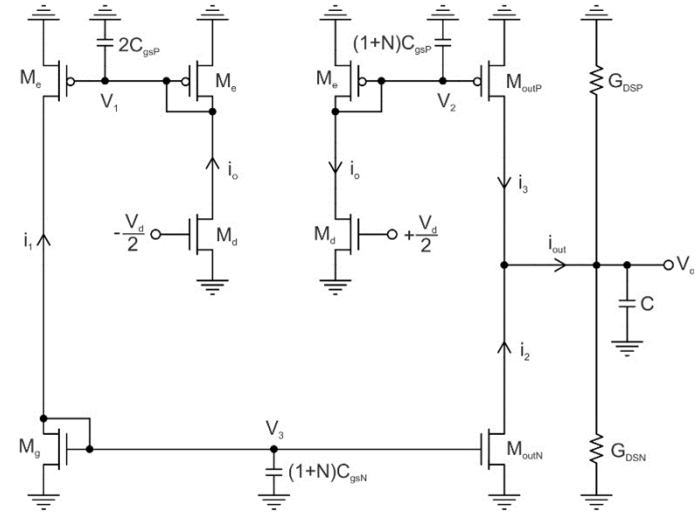
↑
Capacitor de saída define o polo dominante, e faz a compensação em frequência.

N>1

$$V_0 = \frac{\frac{Ngm_d}{(NG_{DS_P} + NG_{DS_N})}}{\left(s \frac{C}{NG_{DS_P} + NG_{DS_N}} + 1 \right)} V_d \rightarrow$$

$$R_0 = \frac{1}{G_{DS_P} + G_{DS_N}}$$

$$\frac{V_0}{V_d} = \frac{R_0 gm_d}{(s R_0 C + 1)}$$

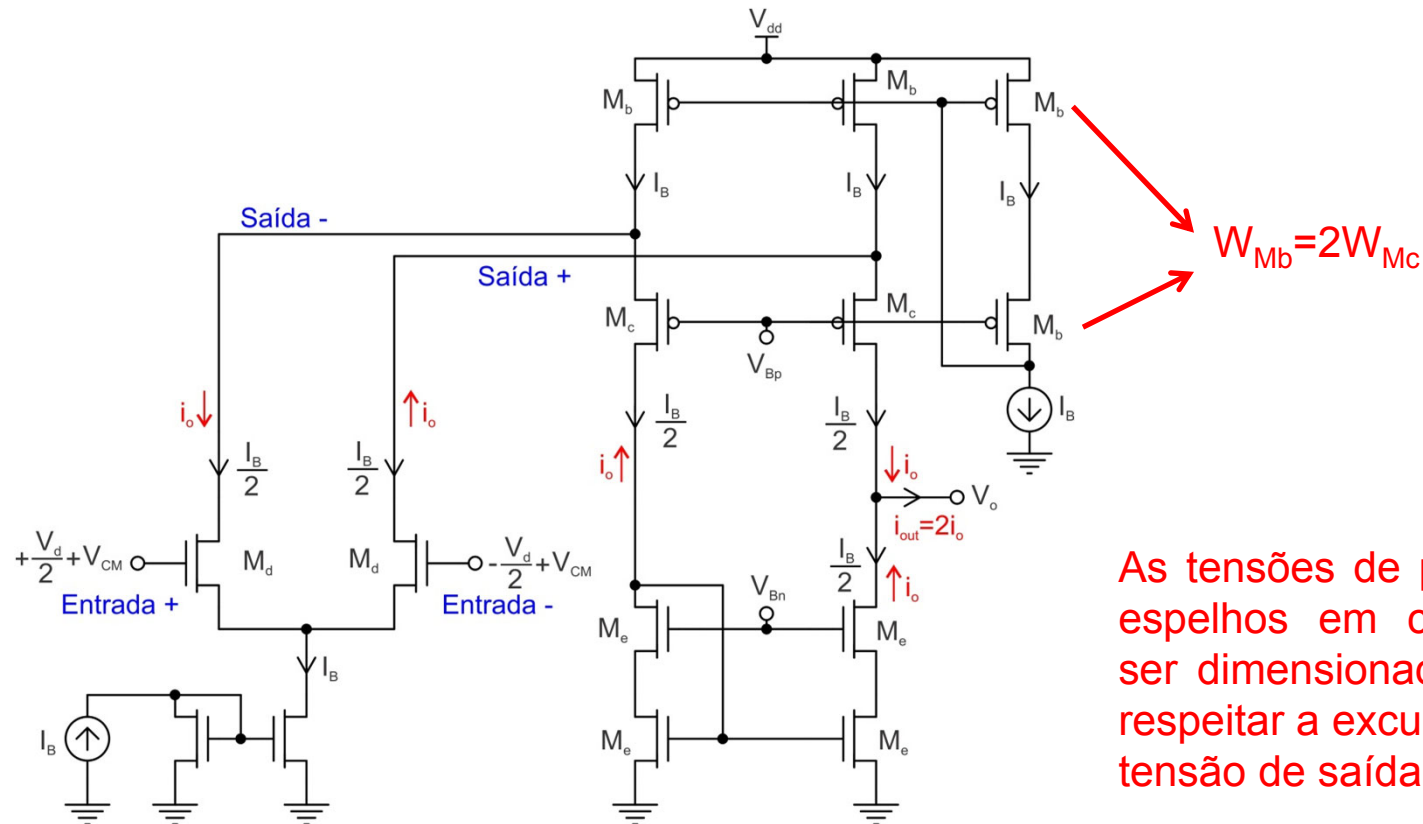


$$\frac{V_0}{V_d} = \frac{R_0 gm_d}{\left(s \frac{R_0 C}{N} + 1 \right)}$$

OTA com Saída em Cascode Dobrado

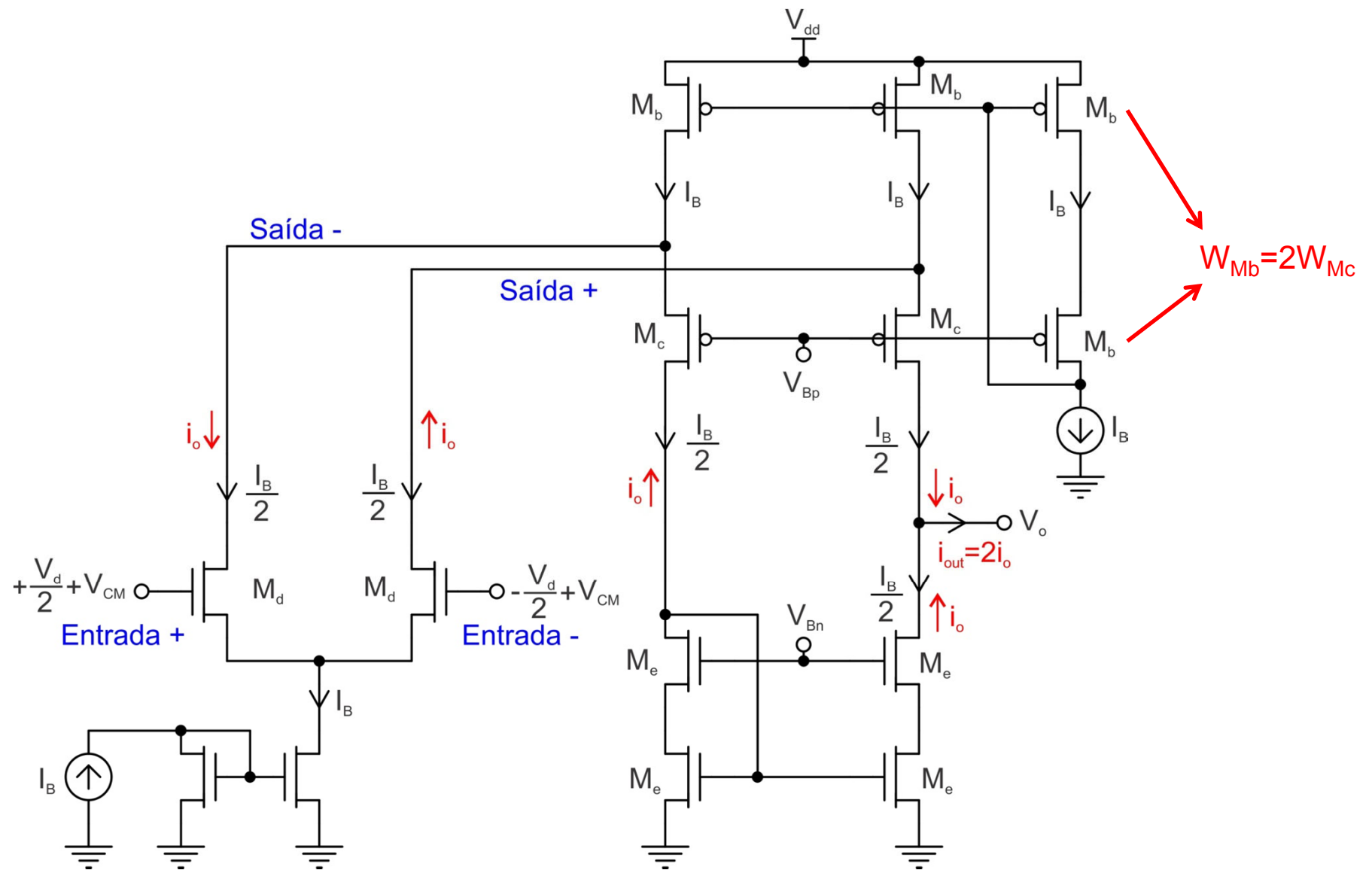
O OTA com estágio de saída em cascode dobrado possui impedância de saída muito mais elevada que a versão simples, e, conseqüentemente, ganho DC mais alto. Esta configuração é a mais usada no projeto de filtros gm-C e capacitores chaveados.

Versão single-ended - NMOS

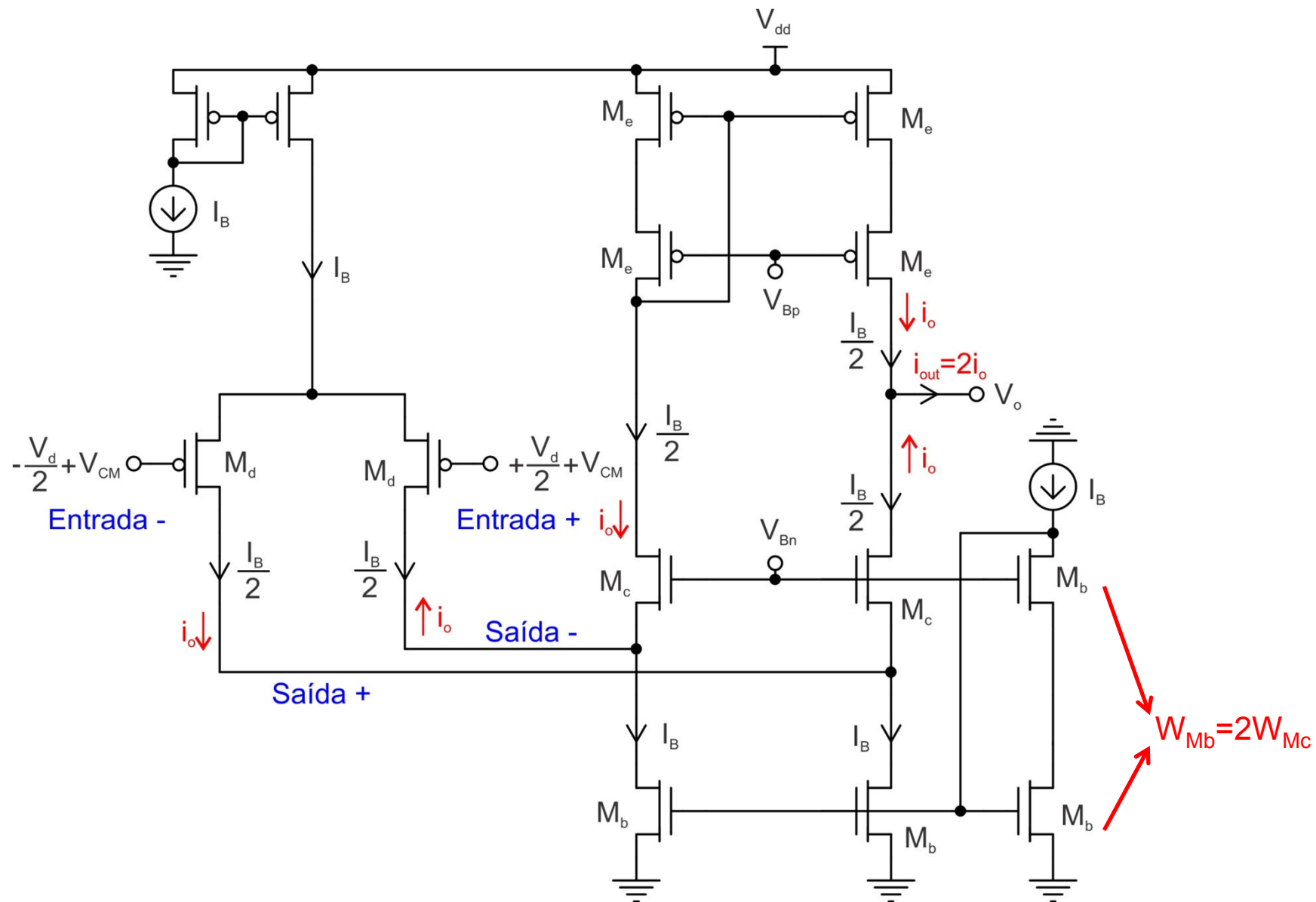


As tensões de polarização dos espelhos em cascode devem ser dimensionadas de forma a respeitar a excursão de sinal de tensão de saída

Princípio de funcionamento da versão single-ended - NMOS

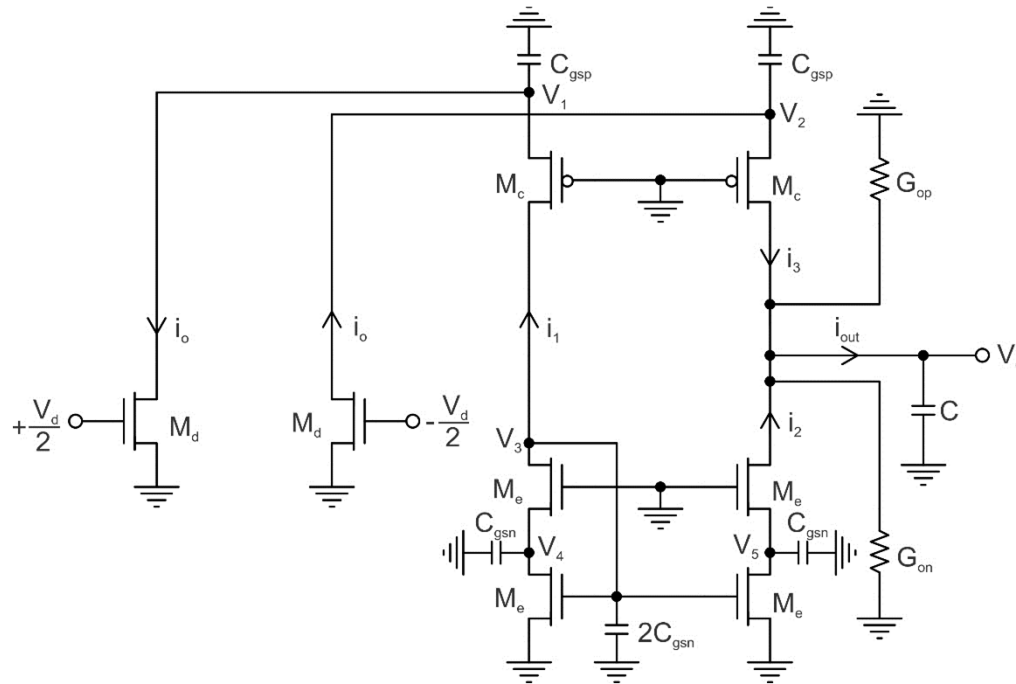


Versão single-ended - PMOS



Análise de Pequenos Sinais com Carga Capacitiva

Versão single-ended - NMOS



$$I_{out} = I_2 + I_3$$

$$I_0 = \frac{gm_d}{2} V_d$$

$$I_1 = \frac{I_0}{s \frac{C_{gs_P}}{gm_c} + 1}$$

$$I_3 = \frac{I_0}{s \frac{C_{gs_P}}{gm_c} + 1}$$

$$I_2 = \frac{I_0}{\left(s^2 \frac{2C_{gs_N}^2}{gm_e^2} + s \frac{2C_{gs_N}}{gm_e} + 1 \right) \left(s \frac{C_{gs_P}}{gm_c} + 1 \right)}$$

$$\frac{I_{out}}{V_d} = \frac{gm_d \left(s^2 \frac{2C_{gs_N}^2}{gm_e^2} + s \frac{2C_{gs_N}}{gm_e} + 2 \right)}{2 \left(s^2 \frac{2C_{gs_N}^2}{gm_e^2} + s \frac{2C_{gs_N}}{gm_e} + 1 \right) \left(s \frac{C_{gs_P}}{gm_c} + 1 \right)}$$

$$\frac{I_{out}}{V_d} = \frac{gm_d \left(s^2 \frac{2C_{gs_N}^2}{gm_e^2} + s \frac{2C_{gs_N}}{gm_e} + 2 \right)}{2 \left(s^2 \frac{2C_{gs_N}^2}{gm_e^2} + s \frac{2C_{gs_N}}{gm_e} + 1 \right) \left(s \frac{C_{gs_P}}{gm_c} + 1 \right)}$$

$$V_0 = \frac{\frac{I_{out}}{(G_{op} + G_{on})}}{\left(s \frac{C}{G_{op} + G_{on}} + 1 \right)}$$

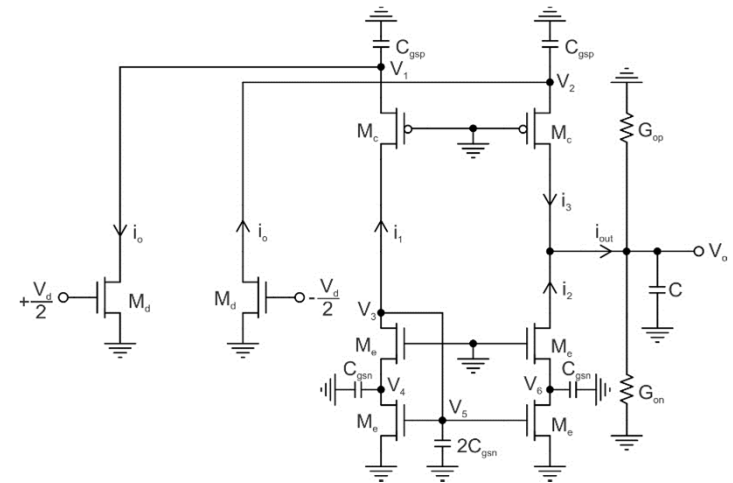
$$\frac{V_0}{V_d} = \frac{\frac{gm_d}{(G_{DS_P} + G_{DS_N})} \left(s^2 \frac{2C_{gs_N}^2}{gm_e^2} + s \frac{2C_{gs_N}}{gm_e} + 2 \right)}{2 \left(s^2 \frac{2C_{gs_N}^2}{gm_e^2} + s \frac{2C_{gs_N}}{gm_e} + 1 \right) \left(s \frac{C_{gs_P}}{gm_c} + 1 \right) \left(s \frac{C}{G_{op} + G_{on}} + 1 \right)}$$

$$gm_e \gg G_{op} + G_{on}$$

$$gm_c \gg G_{op} + G_{on}$$

$$R_0 = \frac{1}{G_{op} + G_{on}}$$

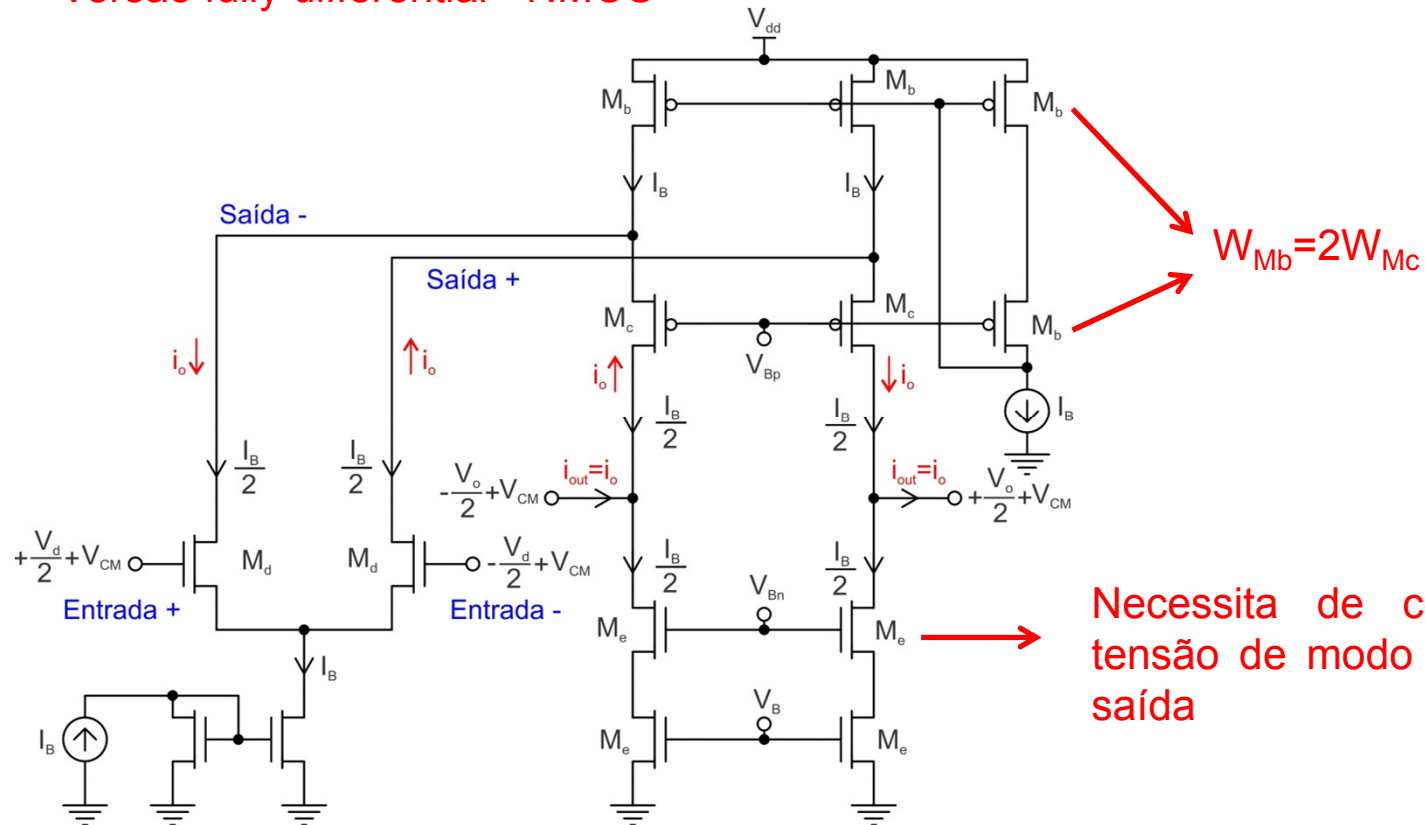
$$\frac{V_0}{V_d} = \frac{R_0 gm_d}{(sR_0 C + 1)}$$



Capacitor de saída define o polo dominante, e faz a compensação em frequência.

OTA com Saída em Cascode Dobrado Fully Differential

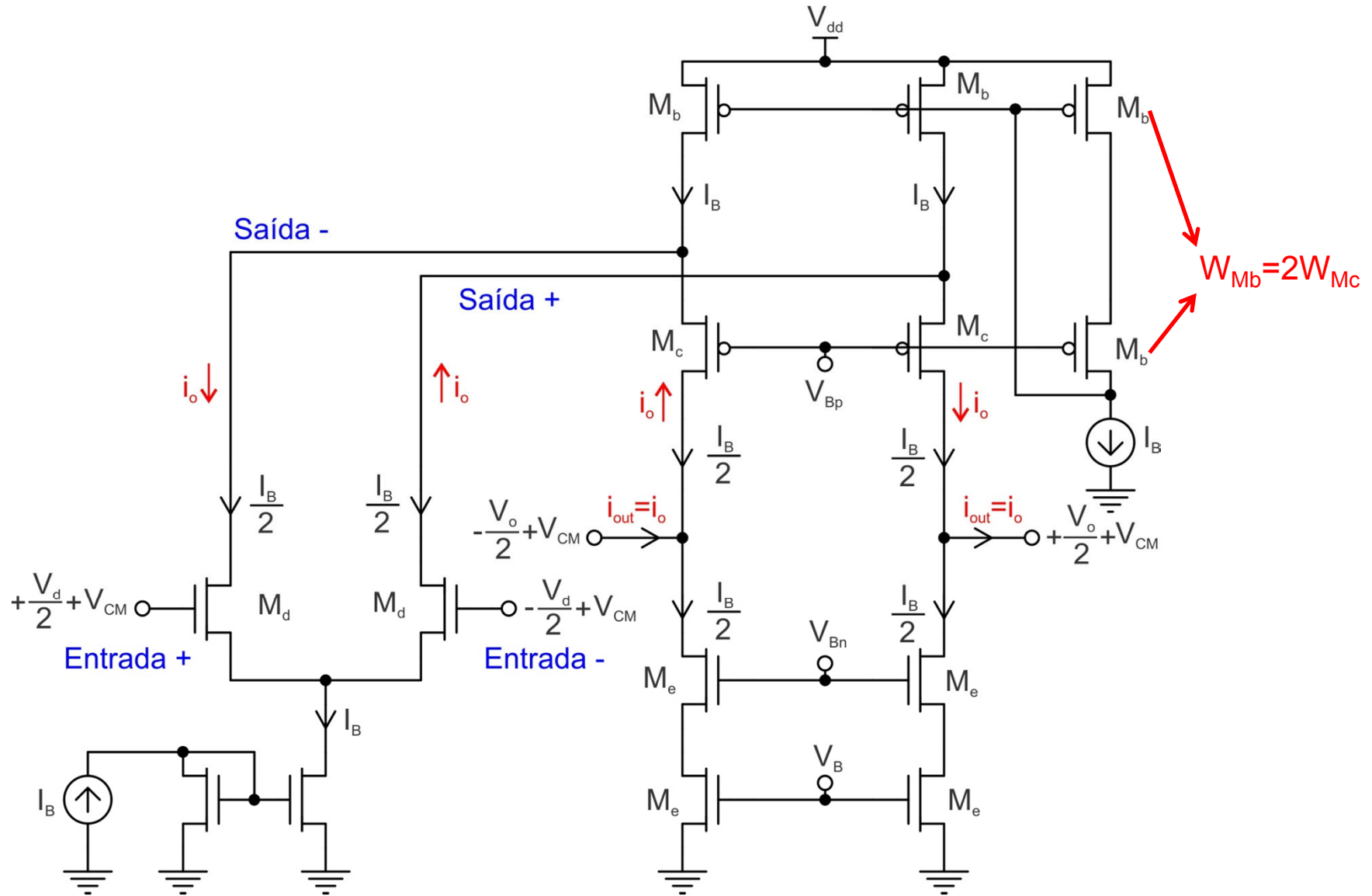
Versão fully differential - NMOS



Necessita de controle de tensão de modo comum na saída

- Menor THD
- Melhor resposta em frequência
- Maior excursão de sinal de tensão de saída
- Maior rejeição de modo comum

Princípio de funcionamento da versão fully differential - NMOS

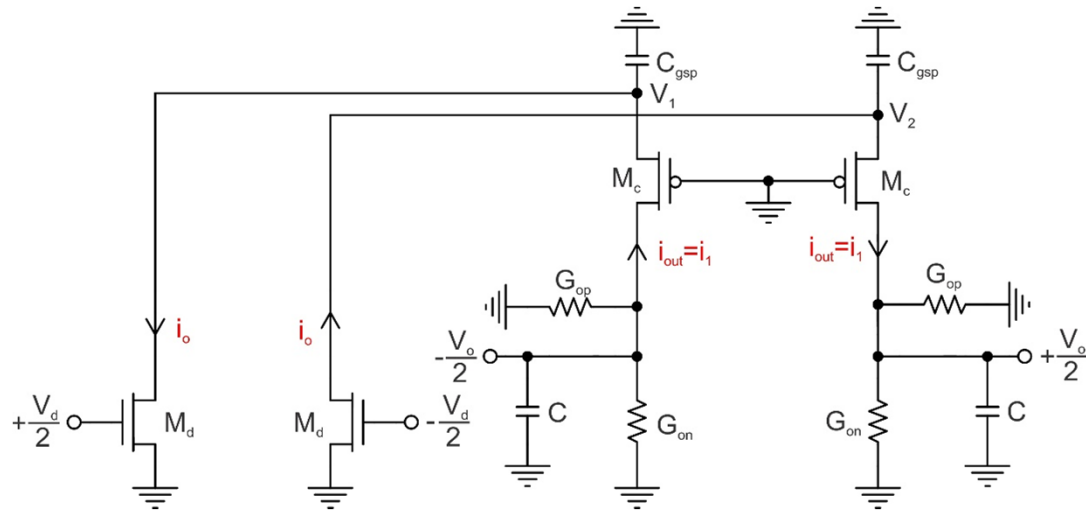


The diagram illustrates a 2.5V CMOS operational amplifier. The input stage is a folded cascode configuration. It features a PMOS differential pair (M_d) with a tail current source I_B connected to ground. The NMOS cascode transistors (M_c) are biased with a current $I_B/2$. The output of the first stage is taken from the PMOS node, which is biased at V_{Bp} . The second stage is a common-source stage with a PMOS load transistor (M_b) and an NMOS driver transistor (M_b). The load transistor is biased with a current I_B . The output of the second stage is taken from the PMOS node, which is biased at V_{Bn} . The output voltage V_o is taken from the PMOS node. The circuit is biased with a tail current I_B and a reference voltage V_{REF} . The output voltage V_o is also shown as a function of the input voltage V_{in} and the output voltage V_o .





Análise AC de Pequenos Sinais com Carga Capacitiva



$$I_0 = \frac{gm_d}{2} V_d$$

$$I_1 = \frac{I_0}{s \frac{C_{gs_P}}{gm_c} + 1}$$

$$I_1 = \frac{gm_d}{s \frac{C_{gs_P}}{gm_c} + 1} \frac{V_d}{2}$$

$$I_{out} = I_1$$

$$\frac{I_{out}}{V_d} = \frac{\frac{gm_d}{2}}{s \frac{C_{gs_P}}{gm_c} + 1} \rightarrow \frac{V_0}{V_d} = \frac{\frac{gm_d}{G_{op} + G_{on}}}{\left(s \frac{C_{gs_P}}{gm_c} + 1 \right) \left(s \frac{C}{G_{op} + G_{on}} + 1 \right)}$$

$$gm_c \gg G_{op} + G_{on} \rightarrow R_0 = \frac{1}{G_{op} + G_{on}} \rightarrow \frac{V_0}{V_d} = \frac{R_0 gm_d}{(s R_0 C + 1)}$$

**Final deste
Tópico**