ELETRÔNICA IV

Apostila de Aulas Práticas

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1. Introdução

O conteúdo desta apostila consiste das aulas experimentais do curso de Eletrônica IV, ministrado no Departamento de Eletrônica da Escola de Engenharia. Cada capítulo corresponde a um experimento a ser montado e estudado em laboratório. Esses experimentos foram, ao longo dos anos, sendo aprimorados didaticamente, de forma a apresentar ao aluno a constatação experimental dos conceitos básicos, e essenciais, estudados na disciplina teórica. Também são fornecidos todos os manuais dos componentes usados nos experimentos, disponibilizando ao aluno todas as informações necessárias à realização dos projetos.

2. AMPLIFICADOR "PUSH-PULL" COM SAÍDA COMPLEMENTAR

ASSUNTO

Projeto de um amplificador de potência, classe AB, com transistores de saída em simetria complementar.

OBJETIVO

Familiarizar o aluno com as condições de operação e características particulares do circuito.

PROJETO

Fase 1- Projete o circuito da Figura 2.1 obedecendo as seguintes especificações:

- 1 Potência C.A. de saída de 1W.
- **2** Carga de 8.2Ω.
- 3 Eficiência superior a 40%.
- 4 Frequência de corte inferior menor que 50Hz.
- 5 Ganho de tensão o maior possível.
- 6 Considerar nos cálculos os transistores: TIP29C, TIP30C, BC547 e BC557 (ou similares).
- 7 Ajuste P1 até obter a tensão DC no ponto A igual a zero.

	COMPONENTES CALCULADOS	8
R3 =	P =	
R4 =	C1 =	
R5 =	C3 =	
	POLARIZAÇÃO	
Teórico	Simulado	Prático
$V_{Bq_Q_1} =$	$V_{Bq_Q_1} =$	$V_{Bq_Q_1} =$
$V_{Bq_Q_5} =$	$V_{Bq_Q_5} =$	$V_{Bq_Q_5} =$
$V_{Bq_2Q_3} =$	$V_{Bq_2Q_3} =$	$V_{Bq_2Q_3} =$
$V_{oq} =$	$V_{oq} =$	$V_{oq} =$
$I_{Cq_Q_S} =$	$I_{Cq_Q_5} =$	$I_{Cq_Q_S} =$
	GANHO DE TENSÃO	·
Teórico	Simulado	Prático
EXCURSÃO I	DE SINAL MÁXIMA NA SAÍDA (2	Sem Saturação)
Teórico	Simulado	Prático

		5
	FREQUÊNCIAS DE CO	RTE
Teórico	Simulado	Prático
Inferior =	Inferior =	Inferior =
	Superior =	Superior =
POT	ÊNCIA MÁXIMA DE SAÍDA ((Sem Saturação)
Teórico	Simulado	Prático
Evolique a função dos se	quintes componentes do circuit	to: R. R. D. D. D. D. C. C. A.C.
	Sumes componentes do en cun	$\mathbf{x}_1, \mathbf{x}_2, \mathbf{p}_1, \mathbf{p}_2, \mathbf{p}_3, \mathbf{p}_4, \mathbf{c}_3, \mathbf{c}_2 \in \mathbf{c}_5$
COME	NTÁRIOS SOBRE OS RESUL	TADOS OBTIDOS
COML		

COMENTÁRIOS SOBRE OS RESULTADOS OBTIDOS

Fase 2- Projete o circuito da Figura 2.2 obedecendo as seguintes recomendações:

^{1 -} Conservar os valores dos componentes calculados para o circuito da Figura 2.1, exceto o capacitor C_1 .

- 2 Identificar o tipo de realimentação empregada.
- 3 Calcular R₆ para se obter um ganho de tensão realimentado de 4. Este ganho é necessário para que um sinal de entrada com 1V de amplitude produza potência máxima na saída do amplificador. Esta é uma especificação comum aos amplificadores de potência comerciais.
- 4 Recalcular C1 para manter a frequência de corte inferior menor que 50Hz.

	COMPONENTES CALCULADOS	5
R6 =	C1 =	
	POLARIZAÇÃO	
Teórico	Simulado	Prático
$V_{Bq_Q_1} =$	$V_{Bq_Q_1} =$	$V_{Bq_Q_1} =$
$V_{Bq_Q_5} =$	$V_{Bq_Q_5} =$	$V_{Bq_Q_S} =$
$V_{Bq_Q_3} =$	$V_{Bq_2Q_3} =$	$V_{Bq_Q_3} =$
$V_{oq} =$	$V_{oq} =$	$V_{oq} =$
$I_{Cq_Q_5} =$	$I_{Cq_Q_5} =$	$I_{Cq_Q_5} =$
Ident	ificar o tipo de realimentação empr	egada
	CANHO DE TENSÃO	
Teórico	Simulado	Prático
	Sinuau	Traceo
EXCU	JRSÃO DE SINAL MÁXIMA NA S	SAÍDA
Teórico	Simulado	Prático
	FREQUÊNCIAS DE CORTE	1
Teórico	Simulado	Prático
Inferior =	Inferior =	Inferior =
	Superior =	Superior =
	POTÊNCIA MÁXIMA DE SAÍDA	
Teórico	Simulado	Prático
	EFICIÊNCIA COM V ₀ =4V _P	1
Teórico	Simulado	Prático

Curto-circuitar os pontos B e C, e esboçar a forma de onda de saída, comparando com a anterior

COMENTÁRIOS SOBRE OS RESULTADOS OBTIDOS

- 1 Monte o circuito da Figura 2.3 (a) utilizando um microfone de eletreto e um resistor $R_{10}=10k\Omega$.
- 2 Fale ao microfone e observe a amplitude máxima do sinal AC em V_{mic}.
- **3** Com a tensão V_{mic}, projete o pré-amplificador da Figura 2.3 (b) de tal forma a se obter uma tensão máxima V_{pre}=1V e frequência de corte inferior menor que 50Hz. Conecte o pré-amplificador ao amplificador da Fase 2, conforme a Figura 2.4, substitua a carga R_L por um alto-falante de 8Ω e fale ao microfone.

	COMPONENTES CALCULADOS	
R7 =	R8 =	C4 =
COMENTA	RIOS SOBRE OS RESULTADOS	OBTIDOS



Figura 2.1: Amplificador Push-Pull.



Figura 2.2: Amplificador Push-Pull com realimentação.



Figura 2.3: Microfone de eletreto. a) Polarização. b) Microfone mais amplificador.



Figura 2.4: Amplificador Push-Pull mais microfone de eletreto.



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3. AMPLIFICADOR SINTONIZADO

OBJETIVO

Estudo de um amplificador sintonizado e sua aplicação como amplificador seletivo e "mixer".

PROJETO

Fase 1- Caracterização da bobina

I - Medir a relação de espiras N_1/N_2 dos indutores, aplicando um sinal senoidal de 100kHz. Considere $N_1 > N_2$.



2 - Medir os parâmetros do indutor, utilizando o esquema abaixo,



onde:

 C_V é uma década capacitiva;

 C_p é a capacitância parasita, que inclui a capacitância do osciloscópio, da fiação, residual da década e da própria bobina;

 R_p é a resistência parasita em paralelo com a bobina.

- **3** Ajuste a frequência do gerador de sinais em 450kHz. Varie a capacitância da década até que o circuito esteja o mais próximo possível da sintonia, e anote o valor obtido C_{V1} . Faça o ajuste fino da frequência do gerador, até obter o ponto exato de sintonia, e anote o valor desta frequência f_1 .
- 4 Ainda com o circuito sintonizado, meça o ganho de tensão $A = V_o/V_{in}$ e calcule R_p .

$$A = \frac{R_p}{R_p + 10k} \quad \rightarrow \quad R_p = \left(\frac{A}{1 - A}\right) 10k$$

- 5 Ajuste a frequência do gerador de sinais em 350kHz. Varie a capacitância da década até que o circuito esteja o mais próximo possível da sintonia, e anote o valor obtido C_{V2} . Faça o ajuste fino da frequência do gerador, até obter o ponto exato de sintonia, e anote o valor desta frequência f_2 .
- 6 Calcule L_1 e C_p através do sistema de equações:

$$\begin{cases} f_1 = \frac{1}{2\pi\sqrt{L_1(C_p + C_{V1})}} \\ f_2 = \frac{1}{2\pi\sqrt{L_1(C_p + C_{V2})}} \end{cases} \rightarrow \begin{cases} L_1 = \frac{f_1^2 - f_2^2}{4\pi^2 f_1^2 f_2^2 (C_{V2} - C_{V1})} \\ C_p = \frac{C_{V2} f_2^2 - C_{V1} f_1^2}{f_1^2 - f_2^2} \end{cases}$$

7 - Calcule o fator de qualidade do indutor na frequência f_1 .

$$Q_b = \frac{R_p}{2\pi f_1 L_1}$$

	PARÂ	METROS DO INDUT	OR	
$L_1 =$	$R_p =$	C _p =	Q _b =	$N_1/N_2 =$

Fase 1- Projetar um amplificador sintonizado, tomando por base, a Figura 3.1, com as seguintes características:

- $1 V_{CC} = 10V;$
- 2 Frequência de sintonia $f_0 = 450 kHz$;
- **3** Ganho de tensão na frequência de sintonia $|A(j2\pi f_0)| = 25$;
- 4 Seletividade igual a 10.
- 5 Considere fator de qualidade igual a 60 para os capacitores de poliéster metalizado.

	COMPONENTES	CALCULADOS	
R1 =			
		C1 =	
R2 =		C2 =	
R3 =		C3=	
RL=		05	
	POLARIZ	LAÇAU	
leórico	Simul	ado	Prático
$V_{Bq} =$	$V_{Bq} =$		$V_{Bq} =$
$V_{Eq} =$	$V_{Eq} =$		$V_{Eq} =$
$I_{Cq} =$	$I_{Cq} =$		$I_{Cq} =$
	FREQUÊNCIA I	DE SINTONIA	
Teórico	Simul	ado	Prático
	SELETIVIDADE	DO CIRCUITO	
Teórico	Simul	ado	Prático
		FOLIÊNCIA DE	
GANHO DI	E TENSAO NA FR	EQUENCIA DE	SINTONIA
Teórico	Simul	ado	Prático

DIGA O QUE DEVI	E SER OBSERVADO NA S	SAÍDA, QUANDO O SINAI	L DE ENTRADA FOR:
	Teórico	Simulado	Prático
senoidal de 450kHz			
senoidal de 225kHz			
senoidal de 150kHz			
senoidal de 900kHz			
quadrado de 450kHz			
quadrado de 225kHz			
quadrado de 150kHz			
	COMENTÁRIOS SOBRE	OS RESULTADOS OBTID	OS

Fase 2- Montar um "mixer", modificando o circuito conforme a Figura 3.2

O objetivo deste experimento é mostrar o efeito do batimento de frequências, muito utilizado nos receptores de rádio. Quando dois sinais senoidais, de frequências f_1 e f_2 , são aplicados à base do transistor, e com amplitudes suficientemente elevadas para forçar a operação na região não linear, a corrente de coletor é o somatório de várias senoides com frequências $f_1 - f_2$ e $\sum_{n=0,m=0}^{\infty} (nf_1 + mf_2)$. Caso

uma destas frequências coincida com a sintonia do filtro, esta será amplificada e visível na saída, enquanto as outras serão fortemente atenuadas. Para obter este efeito, desligue o gerador G₂, ajuste a frequência de G₁ em 4MHz e a amplitude para que, no ponto A, exista uma senoide com $1V_{pico}$. Desligue o gerador G₁, ajuste a frequência de G₂ em 4MHz + f_1 (f_1 sendo a sintonia medida para filtro) e a amplitude para que, no ponto A, exista uma senoide com $1V_{pico}$. Ligue os dois geradores e observe o sinal de saída.

FREQUÊNCIA DO) SINAL DE SAÍDA
Teórico	Prático
f =	f =
ESBOCE A FORMA DE ON	DA OBSERVADA NA SAÍDA
COMENTARIOS SOBRE O	S RESULTADOS OBTIDOS



Figura 3.1: Amplificador sintonizado.



Figura 3.2: Amplificador sintonizado como "mixer".

4. MODULADOR DE AMPLITUDE

OBJETIVO

Estudo de um circuito Modulador de Amplitude (AM), e um demodulador AM por detecção de pico de envoltória.

PROJETO

Fase1 - Projeto do modulador

Utilizando o mesmo indutor acoplado da experiência anterior, dimensione o modulador AM de alto nível da Figura 4.1, de forma a atender as especificações abaixo:

- 1 Frequência da portadora igual a 450kHz;
- 2 Frequência de corte inferior, para o sinal modulador, de 50Hz;
- 3 Frequência de corte superior, para o sinal modulador, de 5kHz;
- 4 Máxima excursão de sinal do oscilador, para qualquer nível de sinal de modulação;
- 5 Tensão e polarização no emissor de Q₂ igual a 1V;
- **6** Carga $R_L = 1k\Omega$.
- 7 Considere fator de qualidade igual a 60 para os capacitores de poliéster metalizado.
- 8 Calcular C₆ para frequência de corte de 100kHz.

	PARÂN	METROS DO INDUT	OR	
L ₁ =	R _p =	C _p =	$Q_b =$	$N_1/N_2 =$

	COMPONENTES CALCULADOS	
R1 =	C1 =	
R2 =	C2 =	
R3 =	C3=	
R4=	C4=	
RL=	C6=	
	POLARIZAÇÃO	
Teórico	Simulado	Prático
$Teórico$ $V_{Bq1} =$	$Simulado$ $V_{Bq1} =$	$\begin{array}{c c} & \mathbf{Pr\acute{a}tico} \\ \hline & V_{Bq1} = \end{array}$
$Teórico$ $V_{Bq1} =$ $V_{Eq1} =$	$Simulado$ $V_{Bq1} =$ $V_{Eq1} =$	Prático $V_{Bq1} =$ $V_{Eq1} =$
Teórico $V_{Bq1} =$ $V_{Eq1} =$ $V_{Bq2} =$	Simulado $V_{Bq1} =$ $V_{Eq1} =$ $V_{Bq2} =$	Prático $V_{Bq1} =$ $V_{Eq1} =$ $V_{Bq2} =$
Teórico $V_{Bq1} =$ $V_{Eq1} =$ $V_{Bq2} =$ $V_{Eq2} =$	Simulado $V_{Bq1} =$ $V_{Eq1} =$ $V_{Bq2} =$ $V_{Eq2} =$	Prático $V_{Bq1} =$ $V_{Eq1} =$ $V_{Bq2} =$ $V_{Eq2} =$

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	FREQUÊNCIA DI	E OSCILAÇÃO	
Teórico	Simul	ado	Prático
Máximo Índice de Modula	ção sem Distorção, p	oara um Sinal Mo	odulador Senoidal de 50Hz
Teórico			Prático
Máximo Indice de Modulaç	ão sem Distorção, p	ara um Sinal Mo	dulador Senoidal de 500Hz
Teórico			Prático
Máximo Índias do Modulas	ža sam Distancão na	ve um Sinel Mer	duladar Sanaidal da 5000Uz
	ao sem Distorção, pa		Drático
Teorico		Pratico	
COMENT	ÁRIOS SOBRE OS	RESULTADOS	OBTIDOS

Troque a carga do modulador por um detector de pico de envoltória, conforme a Figura 4.2. Calcule C_L e recalcule R_L para que o demodulador funcione adequadamente dentro da faixa de frequências especificada para o sinal modulador.

COMPONENTES CALCULADOS	
RL =	CL =
	Frequência de corte inferior do Demodulador (pontos de gueda de 3dB)
	Prático
f _{cr} =	
	COMENTARIOS SOBRE OS RESULTADOS OBTIDOS



Figura 4.1: Modulador de amplitude.



Figura 4.2: Modulador AM com detector de pico de envoltória.

5. MULTIPLICADORES ANALÓGICOS

OBJETIVO

Familiarizar o aluno quanto às técnicas de multiplicação de sinais analógicos variantes no tempo e sua aplicação como moduladores em amplitude com e sem portadora, detectores síncronos, detectores de fase, dobradores de frequência, etc.

INTRODUÇÃO

Durante muito tempo a multiplicação analógica foi conseguida através de várias técnicas como:

- método do quadrado da soma usando dispositivos não lineares que apresentem características quadráticas, predominantes ou não, como FET's, diodos ou transistores de junção, seguidos de filtros passa-faixa.
- método do quadrado da soma balanceada, usando os mesmos dispositivos anteriores, mas em circuitos onde a portadora é suprimida (mais de 40dB) ou reduzida (mais de 20dB). Em baixas frequências pode-se simular um dispositivo com características quadráticas com operacionais e redes de realimentação providas de resistores e diodos em série. Para cada tensão de entrada o ganho será diferente e a aproximação por partes poderá ser quadrática.
- método da modulação por largura de pulsos.
- método dos amplificadores logarítmicos.
- método dos amplificadores de transcondutância variável.

A presente prática será sobre os moduladores balanceados de transcondutância variável e com os coletores dos diferenciais cruzados, conhecidos como células de *Gilbert*. Estas células são comuns a vários integrados como multiplicadores de quatro quadrantes, moduladores, etc.

PROJETO

Fase 1 - Projeto do modulador

Montar um circuito modulador em amplitude da Figura 5.1, que possa funcionar como AM DSB e AM DSB SC numa frequência de portadora $\omega_c = 2\pi \times 150 \times 10^3 rad/s$ e frequência da moduladora $\omega_m = 2\pi f_m$, f_m variando de 100Hz a 3kHz. Utilize o modelo da Figura 5.2 para realizar as simulações. C3 deve ser calculado para a frequência de corte de 10Hz, enquanto C1 e C2 dever ser calculados para a frequência de corte de 100Hz.

COMPONENTES CALCULADOS						
C1=	C2=		C3=			
	PC)LARIZAÇ	CÃO (com o potenciôn	netro a meio cu	rso)	
	Teórico		Simulado		Prático	
$V_1 =$	$V_8 =$	V ₁ =	= V ₈ =	$V_1 =$	$V_8 =$	
V ₂ =	V ₁₀ =	V ₂ =	= V ₁₀ =	$V_2 =$	V ₁₀ =	
V ₃ =	V ₁₂ =	V ₃ =	= V ₁₂ =	V ₃ =	V ₁₂ =	
V4=	$V_5 =$	V ₄ =	= V ₅ =	$V_4=$	V ₅ =	
V ₆ =		V ₆ =	=	$V_6 =$		

Utilize como portadora uma onda senoidal de 150kHz com 500mV de amplitude, e uma senoide de 2kHz e 200mV de amplitude para a moduladora. Ajuste o potenciômetro para que o sinal observado em V_{o+} ou V_{o-} esteja modulado em amplitude e com portadora suprimida.

ESBOCE O SINAL OBSERVADO EM V ₀₊ ou V ₀₋		
Simulado	Prático	

Varie o potenciômetro e observe a modulação mudar gradativamente de <u>portadora suprimida</u> para <u>com portadora</u>.

ESBOCE O SINAL OBSERVADO EM V0+ 00 V0-, COM ÍNDICE DE MODULAÇÃO		
Igual a 50%		

Ajuste o potenciômetro para obter índice de modulação de 100%. Varie a frequência do sinal modulador e, observando a forma do sinal de saída, determine a frequência de corte inferior do modulador.

FREQUÊNCIA DE CORTE INFERIOR DO MODULADOR		
Teórico	Prático	
$\mathbf{f}_{\mathrm{CI}} =$	$\mathbf{f}_{\mathrm{CI}} =$	
COMENTÁRIOS SOBRE OS	RESULTADOS OBTIDOS	

O modulador balanceado pode ser usado, quando o sinal de entrada é senoidal, como duplicador, ou oitavador, de frequência. Para isto, basta aplicar V_{in} simultaneamente às entradas <u>portadora</u> e <u>moduladora</u>. Desta forma, o sinal observado nas saídas V_{o^+} ou V_{o^-} é proporcional a V_{in}^2 , e pode ser representado como:

$$V_{in}^{2}(t) = V_{m} \sin(\omega_{0}t)^{2} = V_{m}^{2} (1 - \cos(2\omega_{0}t))/2$$

Ajuste o potenciômetro para que não exista portadora nas saídas $V_{o+} e V_{o-}$, e aplique um sinal senoidal com 1.5kHz e 50mV de amplitude às entradas portadora e moduladora.

ESBOCE O SINAL OBSERVADO EM V0+ 01 V0-, E ANOTE A FREQUÊNCIA MEDIDA		
Teórico	Simulado	Prático
f=	f=	f=
COMENTA	ÁRIOS SOBRE OS RESULTADOS	OBTIDOS

Fase 3 - Detector de fase

O modulador balanceado pode ser usado como detector de fase, entre dois sinais de mesma frequência, conforme a Figura 5.4. A tensão $V_0(t)$ é o produto $V_1(t) \times V_2(t)$, e considerando estas tensões senoidais, tem-se:

$$V_0(t) = kV_1\sin(\omega_0 t)V_2\sin(\omega_0 t + \theta) = kV_1V_2\cos(\theta)/2 - kV_1V_2\cos(2\omega_0 t + \theta)/2 \rightarrow k \text{ é uma constante}$$

Calculando R e C para que formem um filtro passa-baixas, com frequência de corte suficientemente pequena para eliminar a componente $kV_1V_2\cos(2\omega_0t+\theta)/2$, obtém-se:

$$V_o(t) \cong k V_1 V_2 \cos(\theta) / 2 = V_\theta \cos(\theta)$$

Utilize $V_1(t)$ e $V_2(t)$ com frequência de 5kHz e amplitude de 200mV, e faça o gráfico da tensão de saída versus a fase $V_0 \times \theta = (V_{0+} - V_{0-}) \times \theta$, com a fase variando num passo de 10°. Calcule o capacitor *C* para que a frequência de corte seja menor que 200Hz.





Figura 5.1: Modulador balanceado.



Figura 5.2: Modelo da célula de Gilbert para simulação.



Figura 5.3: Detector de fase.



Figura 5.4: Implementação do detector de fase.

6. MODULADOR DE FM

OBJETIVO

Estudo de um circuito Modulador de Frequência (FM), e determinação do desvio de frequência pelo método do apagamento de portadora.

PROJETO

Fase 1 - Projeto do modulador

Projetar o circuito modulador de FM da Figura 6.1, para operar com frequência de portadora igual a 30MHz. O nível DC da tensão V_a deve ser igual a 6V e a função de transferência $H(s) = V_a/V_{in}$ deve possuir frequência de corte inferior igual a 50Hz e superior igual a 100kHz. O indutor deve ser construído com fio rígido esmaltado de 0.5mm de diâmetro, enrolado em uma fôrma de 1cm de diâmetro e 1.5cm de comprimento. Para o dimensionamento do indutor, utilize a fórmula abaixo:

$$L = \frac{0.394r^2N^2}{9r + 10h}$$

onde

L - é a indutância em μ H.

r - é o raio da bobina em cm.

N - é o número de espiras.

h - é o comprimento da bobina em cm.

COMPONENTES CALCULADOS		
C1=	C2=	C3=
R1=	R2=	R3=

Fase 2 - Medida da constante ko do VCO

No modulador de FM, a frequência é definida pela expressão $\omega(t) = \omega_0 + 2\pi \cdot \Delta f \cdot f(t)$, onde Δf é o desvio de frequência e f(t) é o sinal modulador. Na sua forma canônica, o sinal modulador possui as seguintes características: $\max |f(t)| = 1$ e $\overline{f(t)} = 0$. Portanto, na saída do modulador de FM devemos ter $v_o(t) = A_C \cos \left(\omega_0 t + 2\pi \cdot \Delta f \cdot \int_t f(\tau) d\tau \right)$. No circuito real, a tensão de saída é dada por $v_o(t) = A_C \cos \left(\omega_0 t + 2\pi \cdot k_o \cdot \int_t v_{in}(\tau) d\tau \right)$ Ao aplicarmos $v_{in}(t) = V_m \cos(2\pi \cdot f_m \cdot t)$, obtemos $v_o(t) = A_C \cos \left(\omega_0 t + 2\pi \cdot V_m k_o / f_m \cdot \sin(2\pi \cdot f_m \cdot t) \right)$, onde o termo $V_m k_o$ é o desvio de frequência Δf , e $V_m k_o / f_m$ é o índice de modulação β . Quando $\beta = 2.4$, obtemos o primeiro apagamento de portadora, e esta

propriedade é muito utilizada para determinação do desvio de frequência dos moduladores de FM.

Faça $v_{in}(t) = 0$ e, com o auxilio do analisador de espectro, meça a frequência da portadora do modulador.

		27
	FREQUÊNCIA DA PORTADORA	<u>.</u>
Teórico	Simulado	Prático
f ₀ =	f ₀ =	f ₀ =
COMENT	ÁRIOS SOBRE OS RESULTADOS	OBTIDOS

Ajuste o gerador de sinais para a frequência de 25kHz, aumente gradativamente a amplitude de $v_{in}(t)$ e observe o aparecimento das raias laterais. Meça o espaçamento entre as raias.

ESPAÇAMENTO ENTRE AS RAIAS		
Teórico	Prático	
COMENTÁRIOS SOBRE	OS RESULTADOS OBTIDOS	

Continue aumentando a amplitude de $v_{in}(t)$ até obter o primeiro apagamento de portadora, e calcule a constante k_O do VCO.





Figura 6.1: Circuito modulador de FM.

7. FONTES CHAVEADAS

OBJETIVO

Projetar e verificar o funcionamento dos conversores BOOST, BUCK-BOOST e BUCK.

PRÁTICA

a) Conversor Boost

O circuito da Figura 7.1 é um conversor Boost operando no modo descontínuo. Dimensione $R_s e C_s$ de forma a obter $V_s=20V \text{ com } \alpha=0.5$ e uma variação máxima de 0.1V. A tensão V_{CC} deve ser ajustada em 5V, e V_p conforme a Figura 7.2. Assuma uma frequência de chaveamento de 15kHZ.

Equações de projeto:

Tempo de carregamento do indutor L, $T_C = \alpha T$, $\theta \le \alpha \le 0.5$.

Tempo de descarregamento do indutor L, $T_D = \alpha_I T$, $0 \le \alpha_I \le (1 - \alpha)$.

Tensão de saída $V_s = (V_{CC} - V_T)\alpha/\alpha_1 - V_D + V_{CC}$, onde V_T e V_D são as tensões de condução do transistor e diodo D₁ respectivamente.

Corrente média na carga $I_s = (V_{CC} - V_T) \alpha \alpha_1 T / 2L$.

Corrente máxima acumulada no indutor L, $I_{L_{\text{max}}} = \alpha (V_{CC} - V_T)T/L$.

Capacitor em função da máxima variação de tensão na saída, $C_s = I_s (2 - \alpha_1)^2 T / 4\Delta V_s$.

TENSÃO DE SAÍDA V _s , COM O RESISTOR DE 100Ω EM CURTO-CIRCUITO		
Teórico	Simulado	Prático
V _S =	V _S =	V _S =
TENSÃO DE RIPPLE Δ	Vs, COM O RESISTOR DE 100Ω	EM CURTO-CIRCUITO
Teórico	Simulado	Prático
$\Delta V_{S} =$	$\Delta V_{S} =$	$\Delta V_S =$
Esboce a corrente de carga e des	scarga do indutor, observando a ter	são no ponto A. $V_A = V_{CC} - 100I$.
Teórico	Simulado	Prático

Varie α de 0.2 a 0.5, e plote um gráfico de V _S em função de α .		
Simulado	Prático	
COMENTÁRIOS SOBRE	OS RESULTADOS OBTIDOS	









Figura 7.2: Fonte de excitação do conversor Boost.

b) Conversor Buck-Boost

O circuito da Figura 7.3 é um conversor Buck-Boost operando no modo descontínuo. Dimensione R_s e C_s de forma a obter V_s =-20V com α =0.5 e uma variação máxima de 0.1V. A tensão V_{CC} deve ser ajustada em 5V, e V_p conforme a Figura 7.4. Assuma uma frequência de chaveamento de 15kHZ.

Equações de projeto:

Tempo de carregamento do indutor L, $T_C = \alpha T$, $0 \le \alpha \le 0.5$.

Tempo de descarregamento do indutor L, $T_D = \alpha_I T$, $0 \le \alpha_I \le (1-\alpha)$.

Tensão de saída $V_s = -(V_{CC} - V_T)\alpha/\alpha_1 + V_D$, onde V_T e V_D são as tensões de condução do transistor e diodo D respectivamente.

 $I_{S} = \left(\alpha^{2} \left(V_{CC} - V_{T} \right)^{2} T \right) / \left(2 \left(V_{D} - V_{S} \right) L \right)$, onde I_{S} é a corrente DC na carga R_S, e T o período de chaveamento.

Corrente máxima acumulada no indutor L, $I_{L_{\text{max}}} = \alpha (V_{CC} - V_T)T/L$.

Capacitor em função da máxima variação de tensão na saída, $C_s = I_s \left(2 - \alpha_1\right)^2 T / 4\Delta V_s$.

TENSÃO DE SAÍDA V _s , COM O RESISTOR DE 100Ω EM CURTO-CIRCUITO					
Teórico	Simulado	Prático			
V _S =	V _S =	V _S =			
TENSÃO DE RIPPLE Δ	V _s , COM O RESISTOR DE 100Ω	EM CURTO-CIRCUITO			
Teórico	Simulado	Prático			
$\Delta V_{S} =$	$\Delta V_{S} =$	$\Delta V_{S} =$			
Esboce a corrente de carga e	descarga do indutor, observando a	tensão no ponto A. $V_A = 100I$.			
Teórico	Simulado	Prático			
	2 - 0.5				
$varie \alpha$ de 0.2 a 0.5, e piote um granco de v_s em função de α .					

COMENTÁRIOS SOBRE OS RESULTADOS OBTIDOS





Figura 7.3: Conversor Buck-Boost.



Figura 7.4: Fonte de excitação do conversor Buck-Boost.

c) Conversor Buck

O circuito da Figura 7.5 é um conversor Buck. Calcule α e dimensione R_s e C_s de forma a obter V_s=5V com uma atenuação mínima do filtro LC igual a 0.01 na frequência de chaveamento. A tensão V_{CC} deve ser ajustada em 8V, e V_p conforme a Figura 7.6. Assuma uma frequência de chaveamento de 15kHZ. Considere também a possibilidade α poder variar de um valor mínimo de 0.2 a um máximo de 0.8.

Equações de projeto:

Tempo de carregamento do indutor L, $T_C = \alpha T$, $0.2 \le \alpha \le l$.

Tensão de saída $V_s = (V_{CC} - V_T)\alpha - V_D(1 - \alpha)$, onde V_T e V_D são as tensões de condução do transistor e diodo D respectivamente.

Capacitor $C_s = T^2/(4\pi^2 AL)$, onde A é a atenuação do filtro LC na frequência de chaveamento, T é o período de chaveamento.

A corrente mínima na carga I_{Smin} que garante a corrente I_L no indutor maior que zero, com α mínimo é $I_{Smin} = (V_{CC} + V_D - V_T) \alpha_{min} (1 - \alpha_{min}) T/2L$.

O resistor máximo admissível é $R_{S \max} = V_{S \min} / I_{S \min}$.

TENSÃO DE SAÍDA Vs, COM α CALCULADO				
Teórico	Simulado	Prático		
V _S =	V _S =	V _S =		
ATENUAÇA	ÃO A DO FILTRO LC, COM α CA	ALCULADO		
Teórico	Simulado	Prático		
$\Delta V_S =$	$\Delta V_{S} =$	$\Delta V_S =$		
Varie α de 0.	2 a 0.8, e plote um gráfico de V_{S} em	n função de α.		
Teórico Simulado Prático				









Figura 7.6: Fonte de excitação do conversor Buck.

DATASHEETS

High-speed diodes

Product specification

1N4148; 1N4448

FEATURES

- Hermetically sealed leaded glass SOD27 (DO-35) package
- High switching speed: max. 4 ns
- General application
- Continuous reverse voltage: max. 75 V
- Repetitive peak reverse voltage: max. 75 V
- Repetitive peak forward current: max. 450 mA.

APPLICATIONS

• High-speed switching.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{RRM}	repetitive peak reverse voltage		-	75	V
V _R	continuous reverse voltage		_	75	V
I _F	continuous forward current	see Fig.2; note 1	-	200	mA
I _{FRM}	repetitive peak forward current		-	450	mA
I _{FSM}	non-repetitive peak forward current	square wave; T _j = 25 °C prior to surge; see Fig.4			
		t = 1 μs	-	4	A
		t = 1 ms	-	1	A
		t = 1 s	-	0.5	A
P _{tot}	total power dissipation	T _{amb} = 25 °C; note 1	_	500	mW
T _{stg}	storage temperature		-65	+200	°C
Tj	junction temperature		_	200	°C

Note

1. Device mounted on an FR4 printed circuit-board; lead length 10 mm.

DESCRIPTION

The 1N4148 and 1N4448 are high-speed switching diodes fabricated in planar technology, and encapsulated in hermetically sealed leaded glass SOD27 (DO-35) packages.



High-speed diodes

1N4148; 1N4448

ELECTRICAL CHARACTERISTICS

 $T_j = 25 \ ^{\circ}C$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _F	forward voltage	see Fig.3			
	1N4148	I _F = 10 mA	-	1	V
	1N4448	I _F = 5 mA	0.62	0.72	V
		I _F = 100 mA	-	1	V
I _R	reverse current	$V_R = 20 V$; see Fig.5		25	nA
		V_R = 20 V; T_j = 150 °C; see Fig.5	_	50	μA
I _R	reverse current; 1N4448	V_R = 20 V; T_j = 100 °C; see Fig.5	_	3	μA
C _d	diode capacitance	$f = 1 MHz; V_R = 0; see Fig.6$		4	pF
t _{rr}	reverse recovery time	when switched from $I_F = 10$ mA to $I_R = 60$ mA; $R_L = 100 \Omega$; measured at $I_R = 1$ mA; see Fig.7		4	ns
V _{fr}	forward recovery voltage	when switched from $I_F = 50$ mA; $t_r = 20$ ns; see Fig.8	_	2.5	V

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th j-tp}	thermal resistance from junction to tie-point	lead length 10 mm	240	K/W
R _{th j-a}	thermal resistance from junction to ambient	lead length 10 mm; note 1	350	K/W

Note

1. Device mounted on a printed circuit-board without metallization pad.
High-speed diodes

1N4148; 1N4448

GRAPHICAL DATA



High-speed diodes

1N4148; 1N4448



High-speed diodes

1N4148; 1N4448





FEATURES

- Low current (max. 100 mA)
- Low voltage (max. 65 V).

APPLICATIONS

• General purpose switching and amplification.

DESCRIPTION

NPN transistor in a TO-92; SOT54 plastic package. PNP complements: BC556 and BC557.

PINNING

PIN	DESCRIPTION
1	emitter
2	base
3	collector



LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter			
	BC546		_	80	V
	BC547		-	50	V
V _{CEO}	collector-emitter voltage	open base			
	BC546		_	65	V
	BC547		_	45	V
V _{EBO}	emitter-base voltage	open collector			
	BC546		_	6	V
	BC547		_	6	V
I _C	collector current (DC)		-	100	mA
I _{CM}	peak collector current		-	200	mA
I _{BM}	peak base current		-	200	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C; note 1	-	500	mW
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature		_	150	°C
T _{amb}	operating ambient temperature		-65	+150	°C

Note

1. Transistor mounted on an FR4 printed-circuit board.

BC546; BC547

BC546; BC547

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient	note 1	0.25	K/mW

Note

1. Transistor mounted on an FR4 printed-circuit board.

CHARACTERISTICS

 $T_j = 25 \ ^{\circ}C$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _{CBO}	collector cut-off current	I _E = 0; V _{CB} = 30 V	_	-	15	nA
		$I_E = 0; V_{CB} = 30 V; T_j = 150 °C$	-	-	5	μA
I _{EBO}	emitter cut-off current	I _C = 0; V _{EB} = 5 V	_	-	100	nA
h _{FE}	DC current gain	$I_{C} = 10 \ \mu A; \ V_{CE} = 5 \ V;$				
	BC546A	see Figs 2, 3 and 4	_	90	_	
	BC546B; BC547B		_	150	_	
	BC547C		_	270	_	
	DC current gain	I _C = 2 mA; V _{CE} = 5 V;				
	BC546A	see Figs 2, 3 and 4	110	180	220	
	BC546B; BC547B		200	290	450	
	BC547C		420	520	800	
	BC547		110	_	800	
	BC546		110	_	450	
V _{CEsat}	collector-emitter saturation	I _C = 10 mA; I _B = 0.5 mA	_	90	250	mV
	voltage	$I_{\rm C} = 100 \text{ mA}; I_{\rm B} = 5 \text{ mA}$	_	200	600	mV
V _{BEsat}	base-emitter saturation voltage	I _C = 10 mA; I _B = 0.5 mA; note 1	_	700	_	mV
		$I_{\rm C}$ = 100 mA; $I_{\rm B}$ = 5 mA; note 1	-	900	-	mV
V _{BE}	base-emitter voltage	$I_{C} = 2 \text{ mA}; V_{CE} = 5 \text{ V}; \text{ note } 2$	580	660	700	mV
		I _C = 10 mA; V _{CE} = 5 V	_	-	770	mV
C _c	collector capacitance	I _E = i _e = 0; V _{CB} = 10 V; f = 1 MHz	-	1.5	-	pF
C _e	emitter capacitance	$I_{C} = i_{c} = 0; V_{EB} = 0.5 V; f = 1 MHz$	_	11	_	pF
f _T	transition frequency	I _C = 10mA; V _{CE} = 5 V; f = 100 MHz	100	-	-	MHz
F	noise figure	$I_{C} = 200 \ \mu$ A; V _{CE} = 5 V; R _S = 2 kΩ; f = 1 kHz; B = 200 Hz	-	2	10	dB

Notes

- 1. V_{BEsat} decreases by about 1.7 mV/K with increasing temperature.
- 2. V_{BE} decreases by about 2 mV/K with increasing temperature.

BC546; BC547





BC546; BC547



FEATURES

- Low current (max. 100 mA)
- Low voltage (max. 65 V).

APPLICATIONS

• General purpose switching and amplification.

DESCRIPTION

PNP transistor in a TO-92; SOT54 plastic package. NPN complements: BC546 and BC547.

PINNING

PIN	DESCRIPTION
1	emitter
2	base
3	collector



LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter			
	BC556		_	-80	V
	BC557		_	-50	V
V _{CEO}	collector-emitter voltage	open base			
	BC556		_	-65	V
	BC557		_	-45	V
V _{EBO}	emitter-base voltage	open collector	_	-5	V
I _C	collector current (DC)		_	-100	mA
I _{CM}	peak collector current		-	-200	mA
I _{BM}	peak base current		_	-200	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	_	500	mW
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature		_	150	°C
T _{amb}	operating ambient temperature		-65	+150	°C

BC556; BC557

BC556; BC557

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient	note 1	250	K/W

Note

1. Transistor mounted on an FR4 printed-circuit board.

CHARACTERISTICS

 $T_j = 25 \ ^{\circ}C$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _{CBO}	collector cut-off current	$I_E = 0; V_{CB} = -30 V$	-	-1	-15	nA
		$I_E = 0; V_{CB} = -30 \text{ V}; T_j = 150 \text{ °C}$	_	-	-4	μA
I _{EBO}	emitter cut-off current	$I_{\rm C} = 0; V_{\rm EB} = -5 \text{ V}$	-	-	-100	nA
h _{FE}	DC current gain	$I_{C} = -2 \text{ mA}; V_{CE} = -5 \text{ V};$				
	BC556	see Figs 2, 3 and 4	125	-	475	
	BC557		125	-	800	
	BC556A		125	-	250	
	BC556B; BC557B		220	-	475	
	BC557C		420	-	800	
V _{CEsat}	collector-emitter saturation	$I_{C} = -10 \text{ mA}; I_{B} = -0.5 \text{ mA}$	_	-60	-300	mV
	voltage	$I_{\rm C} = -100 \text{ mA}; I_{\rm B} = -5 \text{ mA}$	-	-180	-650	mV
V _{BEsat}	base-emitter saturation voltage	$I_{C} = -10 \text{ mA}; I_{B} = -0.5 \text{ mA}; \text{ note } 1$	-	-750	-	mV
		$I_{C} = -100 \text{ mA}; I_{B} = -5 \text{ mA}; \text{ note } 1$	-	-930	-	mV
V _{BE}	base-emitter voltage	$I_{C} = -2 \text{ mA}; V_{CE} = -5 \text{ V}; \text{ note } 2$	-600	-650	-750	mV
		$I_{C} = -10 \text{ mA}; V_{CE} = -5 \text{ V}; \text{ note } 2$	-	-	-820	mV
C _c	collector capacitance	$I_E = i_e = 0; V_{CB} = -10 V; f = 1 MHz$	-	3	-	pF
C _e	emitter capacitance	$I_{C} = i_{c} = 0; V_{EB} = -0.5 V; f = 1 MHz$	-	10	-	pF
f _T	transition frequency	$I_{C} = -10 \text{ mA}; V_{CE} = -5 \text{ V}; \text{ f} = 100 \text{ MHz}$	100	-	-	MHz
F	noise figure	$I_{C} = -200 \ \mu$ A; V _{CE} = -5 V; R _S = 2 kΩ; f = 1 kHz; B = 200 Hz	-	2	10	dB

Notes

1. V_{BEsat} decreases by about –1.7 mV/K with increasing temperature.

2. V_{BE} decreases by about -2 mV/K with increasing temperature.

BC556; BC557





PNP general purpose transistors

BC556; BC557



NPN medium frequency transistors

FEATURES

- Low current (max. 30 mA)
- Low voltage (max. 20 V).

APPLICATIONS

- HF applications in radio and television receivers
- FM tuners
- Low noise AM mixer-oscillators
- IF amplifiers in AM/FM receivers.

DESCRIPTION

NPN medium frequency transistor in a TO-92; SOT54 plastic package.

PINNING

PIN	DESCRIPTION
1	base
2	emitter
3	collector



Fig.1 Simplified outline (TO-92; SOT54) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter	-	30	V
V _{CEO}	collector-emitter voltage	open base	-	20	V
I _{CM}	peak collector current		-	30	mA
P _{tot}	total power dissipation	$T_{amb} \le 25 \ ^{\circ}C$	_	300	mW
h _{FE}	DC current gain	I _C = 1 mA; V _{CE} = 10 V			
	BF494		67	220	
	BF495		35	125	
f _T	transition frequency	I _C = 1 mA; V _{CE} = 10 V; f = 100 MHz	120	_	MHz

BF494; BF495

NPN medium frequency transistors

BF494; BF495

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter	-	30	V
V _{CEO}	collector-emitter voltage	open base	-	20	V
V _{EBO}	emitter-base voltage	open collector	_	5	V
I _C	collector current (DC)		-	30	mA
I _{CM}	peak collector current		-	30	mA
P _{tot}	total power dissipation	$T_{amb} \le 25 \ ^{\circ}C$; note 1	_	300	mW
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature		-	150	°C
T _{amb}	operating ambient temperature		-65	+150	°C

Note

1. Transistor mounted on an FR4 printed-circuit board.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient	note 1	420	K/W

Note

1. Transistor mounted on an FR4 printed-circuit board.

CHARACTERISTICS

 $T_{amb} = 25 \ ^{\circ}C$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I _{CBO}	collector cut-off current	I _E = 0; V _{CB} = 20 V	_	100	nA
		$I_E = 0; V_{CB} = 20 V; T_{amb} = 150 \ ^{\circ}C$	-	4	μA
I _{EBO}	emitter cut-off current	I _C = 0; V _{EB} = 4 V	-	100	nA
h _{FE}	DC current gain	I _C = 1 mA; V _{CE} = 10 V			
	BF494		67	220	
	BF494B		100	220	
	BF495		35	125	
	BF495B		100	125	
V_{BE}	base-emitter voltage	I _C = 1 mA; V _{CE} = 10 V	650	740	mV
C _{re}	feedback capacitance	I _C = 0; V _{CB} = 10 V; f = 1 MHz	_	1	pF
f _T	transition frequency	$I_{C} = 1 \text{ mA}; V_{CE} = 10 \text{ V}; f = 100 \text{ MHz}$	120	_	MHz

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- Designed for Complementary Use with the TIP30 Series
- 30 W at 25°C Case Temperature
- 1 A Continuous Collector Current
- 3 A Peak Collector Current
- Customer-Specified Selections Available



Pin 2 is in electrical contact with the mounting base.

MDTRACA

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

RATING	SYMBOL	VALUE	UNIT	
	TIP29		80	
Collector bace voltage $(I_{-} = 0)$	TIP29A	V	100	V
$Collector-base voltage (i_E = 0)$	TIP29B	V CBO	120	v
	TIP29C		140	
	TIP29		40	
Collector emitter veltere $(I_{-} = 0)$	TIP29A	V	60	V
$Collector-entitler voltage (I_B = 0)$	TIP29B	VCEO	80	
	TIP29C		100	
Emitter-base voltage		V _{EBO}	5	V
Continuous collector current		Ι _C	1	A
Peak collector current (see Note 1)		I _{CM}	3	A
Continuous base current		Ι _Β	0.4	A
Continuous device dissipation at (or below) 25°C case temperature (see Note 2)		P _{tot}	30	W
Continuous device dissipation at (or below) 25°C free air temperature (see Note	P _{tot}	2	W	
Unclamped inductive load energy (see Note 4)	1/2LI _C ²	32	mJ	
Operating junction temperature range	Тj	-65 to +150	°C	
Storage temperature range	T _{stg}	-65 to +150	°C	
Lead temperature 3.2 mm from case for 10 seconds		TL	250	°C

NOTES: 1. This value applies for $t_p \leq 0.3$ ms, duty cycle $\leq 10\%.$

2. Derate linearly to 150°C case temperature at the rate of 0.24 W/°C.

3. Derate linearly to 150°C free air temperature at the rate of 16 mW/°C.

4. This rating is based on the capability of the transistor to operate safely in a circuit of: L = 20 mH, $I_{B(on)} = 0.4 \text{ A}$, $R_{BE} = 100 \Omega$, $V_{BE(off)} = 0$, $R_S = 0.1 \Omega$, $V_{CC} = 20 \text{ V}$.



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electrical characteristics at 25°C case temperature

	PARAMETER		TEST CONDITI	IONS	MIN	TYP	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C = 30 mA (see Note 5)	I _B = 0	TIP29 TIP29A TIP29B TIP29C	40 60 80 100			V
I _{CES}	Collector-emitter cut-off current	$V_{CE} = 80 V$ $V_{CE} = 100 V$ $V_{CE} = 120 V$ $V_{CE} = 140 V$	$V_{BE} = 0$	TIP29 TIP29A TIP29B TIP29C			0.2 0.2 0.2 0.2	mA
I _{CEO}	Collector cut-off current	$V_{CE} = 30 V$ $V_{CE} = 60 V$	I _B = 0 I _B = 0	TIP29/29A TIP29B/29C			0.3 0.3	mA
I _{EBO}	Emitter cut-off current	V _{EB} = 5 V	$I_{\rm C} = 0$				1	mA
h _{FE}	Forward current transfer ratio	$V_{CE} = 4 V$ $V_{CE} = 4 V$	$I_{\rm C} = 0.2 \text{ A}$ $I_{\rm C} = 1 \text{ A}$	(see Notes 5 and 6)	40 15		75	
V _{CE(sat)}	Collector-emitter saturation voltage	I _B = 125 mA	I _C = 1 A	(see Notes 5 and 6)			0.7	V
V _{BE}	Base-emitter voltage	V _{CE} = 4 V	I _C = 1 A	(see Notes 5 and 6)			1.3	V
h _{fe}	Small signal forward current transfer ratio	V _{CE} = 10 V	I _C = 0.2 A	f = 1 kHz	20			
h _{fe}	Small signal forward current transfer ratio	V _{CE} = 10 V	I _C = 0.2 A	f = 1 MHz	3			

NOTES: 5. These parameters must be measured using pulse techniques, t_p = 300 $\mu s,$ duty cycle \leq 2%.

6. These parameters must be measured using voltage-sensing contacts, separate from the current carrying contacts.

thermal characteristics

	PARAMETER			MAX	UNIT
R _{θJC}	Junction to case thermal resistance			4.17	°C/W
R _{θJA}	Junction to free air thermal resistance			62.5	°C/W

resistive-load-switching characteristics at 25°C case temperature

	PARAMETER	TEST CONDITIONS [†]			MIN	ТҮР	MAX	UNIT
t _{on}	Turn-on time	I _C = 1 A	I _{B(on)} = 0.1 A	$I_{B(off)} = -0.1 A$		0.5		μs
t _{off}	Turn-off time	$V_{BE(off)} = -4.3 V$	$R_L = 30 \ \Omega$	t_p = 20 µs, dc \leq 2%		2		μs

[†] Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

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TYPICAL CHARACTERISTICS



Power D

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MAXIMUM SAFE OPERATING REGIONS





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- Designed for Complementary Use with the TIP29 Series
- 30 W at 25°C Case Temperature
- 1 A Continuous Collector Current
- 3 A Peak Collector Current
- Customer-Specified Selections Available



Pin 2 is in electrical contact with the mounting base.

MDTRACA

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

RATING	SYMBOL	VALUE	UNIT	
	TIP30		-80	
Collector bace veltage $(L = 0)$	TIP30A	V	-100	V
$Collector-base voltage (i_E = 0)$	TIP30B	¢СВО	-120	v
	TIP30C		-140	
	TIP30		-40	
Collector omitter veltage $(I_{-} = 0)$	TIP30A	V	-60	V
$Conector-ennitier voltage (I_B = 0)$	TIP30B	V CEO	-80	
	TIP30C		-100	
Emitter-base voltage	V _{EBO}	-5	V	
Continuous collector current		Ι _C	-1	A
Peak collector current (see Note 1)		I _{CM}	-3	A
Continuous base current		Ι _Β	-0.4	A
Continuous device dissipation at (or below) 25°C case temperature (see Note 2)		P _{tot}	30	W
Continuous device dissipation at (or below) 25°C free air temperature (see Note	P _{tot}	2	W	
Unclamped inductive load energy (see Note 4)	½Ll _C ²	32	mJ	
Operating junction temperature range	Tj	-65 to +150	°C	
Storage temperature range	T _{stg}	-65 to +150	°C	
Lead temperature 3.2 mm from case for 10 seconds		TL	250	°C

NOTES: 1. This value applies for $t_p \leq 0.3$ ms, duty cycle $\leq 10\%.$

2. Derate linearly to 150°C case temperature at the rate of 0.24 W/°C.

3. Derate linearly to 150°C free air temperature at the rate of 16 mW/°C.

4. This rating is based on the capability of the transistor to operate safely in a circuit of: L = 20 mH, $I_{B(on)}$ = -0.4 A, R_{BE} = 100 Ω , $V_{BE(off)}$ = 0, R_S = 0.1 Ω , V_{CC} = -20 V.



Information is current as of publication date. Products conform to specifications in accordance with the terms of Power Innovations standard warranty. Production processing does not necessarily include testing of all parameters.



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electrical characteristics at 25°C case temperature

	PARAMETER		TEST CONDITIO	ONS	MIN	TYP	MAX	UNIT
V _{(BR)CEO}	Collector-emitter	I _C = -30 mA	I _B = 0	TIP30 TIP30A TIP30B	-40 -60 -80			V
	2. oanao mir tonago	(see Note 5)		TIP30C	-100			
		V _{CE} = -80 V	$V_{BE} = 0$	TIP30			-0.2	
loro	Collector-emitter	V _{CE} = -100 V	$V_{BE} = 0$	TIP30A			-0.2	mA
·CES	cut-off current	V _{CE} = -120 V	$V_{BE} = 0$	TIP30B			-0.2	
		V _{CE} = -140 V	$V_{BE} = 0$	TIP30C			-0.2	
lana	Collector cut-off	V _{CE} = -30 V	I _B = 0	TIP30/30A			-0.3	mΑ
'CEO	current	V _{CE} = -60 V	$I_B = 0$	TIP30B/30C			-0.3	IIIA
I _{EBO}	Emitter cut-off current	V _{EB} = -5 V	I _C = 0				-1	mA
h	Forward current	$V_{CE} = -4 V$	I _C = -0.2 A	(see Notes 5 and 6)	40			
''FE	transfer ratio	$V_{CE} = -4 V$	I _C = -1 A	(See Notes 5 and 6)	15		75	
V _{CE(sat)}	Collector-emitter saturation voltage	I _B = -125 mA	I _C = -1 A	(see Notes 5 and 6)			-0.7	V
V _{BE}	Base-emitter voltage	V _{CE} = -4 V	I _C = -1 A	(see Notes 5 and 6)			-1.3	V
h _{fe}	Small signal forward current transfer ratio	V _{CE} = -10 V	I _C = -0.2 A	f = 1 kHz	20			
h _{fe}	Small signal forward current transfer ratio	V _{CE} = -10 V	I _C = -0.2 A	f = 1 MHz	3			

NOTES: 5. These parameters must be measured using pulse techniques, t_p = 300 $\mu s,$ duty cycle \leq 2%.

6. These parameters must be measured using voltage-sensing contacts, separate from the current carrying contacts.

thermal characteristics

	PARAMETER			MAX	UNIT
R _{θJC}	Junction to case thermal resistance			4.17	°C/W
R _{θJA}	Junction to free air thermal resistance			62.5	°C/W

resistive-load-switching characteristics at 25°C case temperature

	PARAMETER	TEST CONDITIONS [†]				TYP	MAX	UNIT
t _{on}	Turn-on time	I _C = -1 A	I _{B(on)} = -0.1 A	$I_{B(off)} = 0.1 A$		0.3		μs
t _{off}	Turn-off time	$V_{BE(off)} = 4.3 V$	$R_L = 30 \Omega$	t_p = 20 µs, dc \leq 2%		1		μs

[†] Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

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MAXIMUM SAFE OPERATING REGIONS





Figure 5.

- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonic Distortion 0.003% Typ

- Low Noise V_n = 18 nV/√Hz Typ at f = 1 kHz
- High Input Impedance . . . JFET Input Stage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- High Slew Rate ... 13 V/μs Typ
- Common-Mode Input Voltage Range
 Includes V_{CC+}

description

The JFET-input operational amplifiers in the TL07_ series are designed as low-noise versions of the TL08_ series amplifiers with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL07_ series ideally suited for high-fidelity and audio preamplifier applications. Each amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from -40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of -55°C to 125°C.

					PA	CKAGE			
TA	V _{IO} max AT 25°C	SMALL OUTLINE (D) [†]	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (N)	PLASTIC DIP (P)	TSSOP PACKAGE (PW)	FLAT PACKAGE (W)
	10 mV 6 mV 3 mV	TL071CD TL071ACD TL071BCD	_	_	_	_	TL071CP TL071ACP TL071BCP	TL071CPWLE — —	_
0°C to 70°C	10 mV 6 mV 3 mV	TL072CD TL072ACD TL072BCD	_	_	_	_	TL072CP TL072ACP TL072BCP	TL072CPWLE — —	_
	10 mV 6 mV 3 mV	TL074CD TL074ACD TL074BCD	_	_	_	TL074CN TL074ACN TL074BCN	_	TL074CPWLE — —	_
-40°C to 85°C	6 mV	TL071ID TL072ID TL074ID	—	_	_	— — TL074IN	TL071IP TL072IP —	—	_
−55°C to 125°C	6 mV 6 mV 9 mV	_	TL071MFK TL072MFK TL074MFK	 TL074MJ	TL071MJG TL072MJG —	 TL074MN	 TL072MP 	_	 TL074MW

AVAILABLE OPTIONS

[†] The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL071CDR). The PW package is only available left-ended taped and reeled (e.g., TL072CPWLE).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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NC – No internal connection

symbols







schematic (each amplifier)



All component values shown are nominal.

COMPONENT COUNT [†]							
COMPONENT TYPE TL071 TL072 TL074							
Resistors	11	22	44				
Transistors	14	28	56				
JFET	2	4	6				
Diodes	1	2	4				
Capacitors	1	2	4				
epi-FET	1	2	4				

[†] Includes bias and trim circuitry



TL071, TL071A, TL071B, TL072 TL072A, TL072B, TL074, TL074A, TL074B LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{CC+} (see Note 1)	
Differential input voltage, V _{CC} (see Note 1)	±30 V
Input voltage, VI (see Notes 1 and 3)	±15 V
Duration of output short circuit (see Note 4)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T _A : C suffix	0°C to 70°C
I suffix	−40°C to 85°C
M suffix	–55°C to 125°C
Storage temperature range	65°C to 150°C
Case temperature for 60 seconds: FK package	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J, JG, or W pa	ackage 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, P, or PW	/ package 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.

2. Differential voltages are at IN+ with respect to IN-.

3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.

4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR	DERATE ABOVE T _A	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING	T _A = 125°C POWER RATING		
D (8 pin)	680 mW	5.8 mW/°C	33°C	465 mW	378 mW	N/A		
D (14 pin)	680 mW	7.6 mW/°C	60°C	604 mW	490 mW	N/A		
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW		
J	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW		
JG	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW		
N	680 mW	9.2 mW/°C	76°C	680 mW	597 mW	N/A		
Р	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A		
PW (8 pin)	525 mW	4.2 mW/°C	70°C	525 mW	N/A	N/A		
PW (14 pin)	700 mW	5.6 mW/°C	70°C	700 mW	N/A	N/A		
W	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	200 mW		





PARAMETER		TEST CON	IDITIONS [†]	т _А ‡		TL071C TL072C TL074C		ר ר ז	L071A0 L072A0 L074A0		ר ר ר	L071BC L072BC	;		TL071I TL072I TL074I		UNIT	
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
Vie	Input offect voltage		$P_{0} = 50.0$	25°C		3	10		3	6		2	3		3	6	m\/	
۷IV	input onset voltage	VO = 0,	KS = 20.75	Full range			13			7.5			5			8		
αΛΙΟ	Temperature coefficient of input offset voltage	V _O = 0,	R _S = 50 Ω	Full range		18			18			18			18		μV/°C	
l. a	logent offerst surmout			25°C		5	100		5	100		5	100		5	100	pА	
NO	Input onset current	vO = 0		Full range			10			2			2			2	nA	
lun.			25°C		65	200		65	200		65	200		65	200	pА		
чВ	input bias currents	AO = 0		Full range			7			7			7			20	nA	
VICR	Common-mode input voltage range			25°C	±11	-12 to 15		±11	-12 to 15		±11	-12 to 15		±11	-12 to 15		V	
Maximum paak	$R_L = 10 \ k\Omega$		25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5				
∨ом	V _{OM} output voltage	$R_L \ge 10 \ k\Omega$			±12			±12			±12			±12			V	
	swing	$R_L \ge 2 k\Omega$		Full range	±10			±10			±10			±10			1	
	Large-signal			25°C	25	200		50	200		50	200		50	200			
AVD	differential voltage amplification	V _O = ±10 V,	$R_L \ge 2 k\Omega$	Full range	15			25			25			25			V/mV	
B ₁	Unity-gain bandwidth			25°C		3			3			3			3		MHz	
r _i	Input resistance			25°C		1012			1012			1012			10 ¹²		Ω	
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}m$ $V_{O} = 0,$	nin, R _S = 50 Ω	25°C	70	100		75	100		75	100		75	100		dB	
ksvr	Supply-voltage rejection ratio $(\Delta V_{CC} \pm / \Delta V_{IO})$	$V_{CC} = \pm 9 V$ $V_{O} = 0,$	to ±15 V, R _S = 50 Ω	25°C	70	100		80	100		80	100		80	100		dB	
ICC	Supply current (each amplifier)	V _O = 0,	No load	25°C		1.4	2.5		1.4	2.5		1.4	2.5		1.4	2.5	mA	
V _{O1} /V _{O2}	Crosstalk attenuation	A _{VD} = 100		25°C		120			120			120			120		dB	

electrical characteristics. $V_{CC} = +15$ V (unless otherwise noted)

[†] All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.

[‡] Full range is $T_A = 0^{\circ}C$ to 70°C for TL07_C,TL07_AC, TL07_BC and is $T_A = -40^{\circ}C$ to 85°C for TL07_I.

§ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 4. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

TL072A, TL072B, TL074, TL074A, TL074B LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

TL071,

TL071A, TL071B,

, TL072

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TL071, TL071A, TL071B, TL072 TL072A, TL072B, TL074, TL074A, TL074B LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

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electrical characteristics, V_{CC \pm} = ±15 V (unless otherwise noted)

PARAMETER		TEST CON	IDITIONS [†]	т _д ‡		TL071M TL072M			UNIT			
					MIN	TYP	MAX	MIN	TYP	MAX		
Vio	Input offset voltage	$V_{0} = 0$	$R_{0} = 50.0$	25°C		3	6		3	9	m\/	
10	input onset voltage	VO = 0,	115 - 50 22	Full range			9			15	IIIV	
αΛΙΟ	Temperature coefficient of input offset voltage	$V_{O} = 0,$	$R_S = 50 \Omega$	Full range		18			18		μV/°C	
lio	Input offect ourrent	Vo = 0		25°C		5	100		5	100	рА	
UU	Input onset current	VO = 0		Full range			20			20	nA	
lin.	Input biog ourrent	$V_{0} = 0$		25°C		65	200		65	200	pА	
чв	Input bias current+	V0-0					50			50	nA	
	Common-mode input					-12			-12			
VICR	voltage range			25°C	±11	to 15		±11	to 15		V	
	Maximum peak output voltage swing	$R_L = 10 \ k\Omega$		25°C	±12	±13.5		±12	±13.5			
Vом		$R_L \ge 10 \ k\Omega$		Full range	±12			±12			V	
		$R_L \ge 2 k\Omega$		i uli lange	±10			±10				
AVD	Large-signal differential	$V_{0} = +10 V$	$R_1 > 2 kO$	25°C	35	200		35	200		\//m\/	
~vD	voltage amplification	VO = ±10 V,			15			15			v/IIIv	
B ₁	Unity-gain bandwidth	$T_A = 25^{\circ}C$				3			3		MHz	
ri	Input resistance	T _A = 25°C				1012			1012		Ω	
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ n $V_{O} = 0$,	nin, R _S = 50 Ω	25°C	80	86		80	86		dB	
k _{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 9 V$ $V_{O} = 0,$	to ±15 V, R _S = 50 Ω	25°C	80	86		80	86		dB	
ICC	Supply current (each amplifier)	V _O = 0,	No load	25°C		1.4	2.5		1.4	2.5	mA	
V ₀₁ /V ₀₂	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB	

† Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 4. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

‡All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range is $T_A = -55^{\circ}C$ to $125^{\circ}C$.



PARAMETER		TEST CONDITIONS		TL07xM			ALL	LINUT		
		TEST CO	STCONDITIONS		TYP	MAX	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V _I = 10 V, C _L = 100 pF,	R _L = 2 kΩ, See Figure 1	5	13		8	13		V/µs
	Rise time overshoot	V _I = 20 mV,	$R_L = 2 k\Omega$,		0.1			0.1		μs
۲	factor	C _L = 100 pF,	See Figure 1		20%			20%		
Vn	Equivalent input noise voltage	$B_{0} = 20.0$	f = 1 kHz		18			18		nV/√Hz
		RS = 20.32	f = 10 Hz to 10 kHz		4			4		μV
I _n	Equivalent input noise current	R _S = 20 Ω,	f = 1 kHz		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	V_{I} rms = 6 V, R _L \ge 2 k Ω , f = 1 kHz	$\begin{array}{l} A_{VD} = 1, \\ R_S \leq 1 \; k\Omega , \end{array} \label{eq:average}$		0.003%		(0.003%		

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25^{\circ}C$

PARAMETER MEASUREMENT INFORMATION



Figure 1. Unity-Gain Amplifier



Figure 2. Gain-of-10 Inverting Amplifier



Figure 3. Input Offset Voltage Null Circuit



TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I _{IB}	Input bias current	vs Free-air temperature	4
Vом	Maximum output voltage	vs Frequency vs Free-air temperature vs Load resistance vs Supply voltage	5, 6, 7 8 9 10
AVD	Large-signal differential voltage amplification	vs Free-air temperature vs Frequency	11 12
	Phase shift	vs Frequency	12
	Normalized unity-gain bandwidth	vs Free-air temperature	13
	Normalized phase shift	vs Free-air temperature	13
CMRR	Common-mode rejection ratio	vs Free-air temperature	14
ICC	Supply current	vs Supply voltage vs Free-air temperature	15 16
PD	Total power dissipation	vs Free-air temperature	17
	Normalized slew rate	vs Free-air temperature	18
Vn	Equivalent input noise voltage	vs Frequency	19
THD	Total harmonic distortion	vs Frequency	20
	Large-signal pulse response	vs Time	21
Vo	Output voltage	vs Elapsed time	22



TYPICAL CHARACTERISTICS[†]



[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



TYPICAL CHARACTERISTICS[†]



⁺ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.











[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



TYPICAL CHARACTERISTICS[†]



[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



TYPICAL CHARACTERISTICS





TYPICAL CHARACTERISTICS



Figure 22





MC1496, B

Balanced Modulators/ Demodulators

These devices were designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection, and chopper applications. See Motorola Application Note AN531 for additional design information.

• Excellent Carrier Suppression -65 dB typ @ 0.5 MHz

-50 dB typ @ 10 MHz

Figure 1. Suppressed

Carrier Output

Waveform

Figure 2. Suppressed

Carrier Spectrum

Figure 3. Amplitude Modulation Output

Waveform

- Adjustable Gain and Signal Handling
- Balanced Inputs and Outputs

20

• High Common Mode Rejection -85 dB typical

= 500 kHz, Is = 1.0 kHz

I_C = 500 kHz I_S = 1.0 kHz

This device contains 8 active transistors.

BALANCED MODULATORS/DEMODULATORS

> SEMICONDUCTOR TECHNICAL DATA





ORDERING INFORMATION

Device	Operating Temperature Range	Package		
MC1496D	T. 000 to 17000	SO-14		
MC1496P	$I_{A} = 0^{\circ}C to + 70^{\circ}C$	Plastic DIP		
MC1496BP	$T_A = -40^{\circ}C$ to $+125^{\circ}C$	Plastic DIP		

Figure 4. Amplitude–Modulation Spectrum




MAXIMUM RATINGS ($T_A = 25^{\circ}C$, unless otherwise noted.)

Rating	Symbol	Value	Unit
Applied Voltage (V6 – V8, V10 – V1, V12 – V8, V12 – V10, V8 – V4, V8 – V1, V10 – V4, V6 – V10, V2 – V5, V3 – V5)	ΔV	30	Vdc
Differential Input Signal	V8 – V10 V4 – V1	+5.0 ±(5+I5R _e)	Vdc
Maximum Bias Current	I5	10	mA
Thermal Resistance, Junction–to–Air Plastic Dual In–Line Package	R _{θJA}	100	°C/W
Operating Temperature Range	ТА	0 to +70	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, V_{EE} = -8.0 Vdc, I5 = 1.0 mAdc, R_L = 3.9 k Ω , R_e = 1.0 k Ω , T_A = T_{low} to T_{high} , all input and output characteristics are single-ended, unless otherwise noted.)

Characteristic	Fig.	Note	Symbol	Min	Тур	Max	Unit
Carrier Feedthrough $f_C = 60 \text{ mVrms sine wave and}$ $f_C = 1.0 \text{ kHz}$ offset adjusted to zero $f_C = 10 \text{ MHz}$ $V_C = 300 \text{ mVpp square wave:}$ $f_C = 1.0 \text{ kHz}$	5	1	VCFT		40 140 0.04	_ _ 0.4	μVrms mVrms
offset not adjusted $f_{C} = 1.0 \text{ kHz}$				-	20	200	
Carrier Suppression $f_S = 10 \text{ kHz}$, 300 mVrms $f_C = 500 \text{ kHz}$, 60 mVrms sine wave $f_C = 10 \text{ MHz}$, 60 mVrms sine wave	5	2	VCS	40	65	_	dB
Transadmittance Bandwidth (Magnitude) (R _L = 50 Ω) Carrier Input Port, V _C = 60 mVrms sine wave $f_S = 1.0 \text{ kHz}$, 300 mVrms sine wave Signal Input Port, V _S = 300 mVrms sine wave	8	8	BW _{3dB}	-	300 80	-	MHz
Signal Gain (Vs = 100 mVrms, f = 1.0 kHz; $ V_C $ = 0.5 Vdc)	10	3	Avs	2.5	3.5	_	V/V
Single–Ended Input Impedance, Signal Port, f = 5.0 MHz Parallel Input Resistance Parallel Input Capacitance	6	-	r _{ip}		200 2.0		kΩ pF
Single–Ended Output Impedance, f = 10 MHz Parallel Output Resistance Parallel Output Capacitance	6	-	r _{op} c _{oo}		40 5.0		kΩ pF
Input Bias Current $I_{bS} = \frac{11 + 14}{2}; I_{bC} = \frac{18 + 110}{2}$	7	-	I _{bS} I _{bC}		12 12	30 30	μΑ
Input Offset Current $I_{ioS} = I1-I4$; $I_{ioC} = I8-I10$	7	-	I _{ioS} I _{ioC}		0.7 0.7	7.0 7.0	μΑ
Average Temperature Coefficient of Input Offset Current $(T_A = -55^{\circ}C \text{ to } +125^{\circ}C)$	7	-	TC _{lio}	-	2.0	-	nA/°C
Output Offset Current (I6–I9)	7	-	I ₀₀	-	14	80	μΑ
Average Temperature Coefficient of Output Offset Current $(T_A = -55^{\circ}C \text{ to } +125^{\circ}C)$	7	-	TC _{loo}	-	90	-	nA/°C
Common–Mode Input Swing, Signal Port, f _S = 1.0 kHz	9	4	CMV	-	5.0	-	Vpp
Common–Mode Gain, Signal Port, f _S = 1.0 kHz, V _C = 0.5 Vdc	9	-	ACM	-	-85	-	dB
Common–Mode Quiescent Output Voltage (Pin 6 or Pin 9)	10	-	Vout	-	8.0	-	Vpp
Differential Output Voltage Swing Capability	10	-	Vout	-	8.0	-	Vpp
Power Supply Current 16 +112 114	7	6	ICC IEE	-	2.0 3.0	4.0 5.0	mAdc
DC Power Dissipation	7	5	PD	-	33	-	mW

GENERAL OPERATING INFORMATION

Carrier Feedthrough

Carrier feedthrough is defined as the output voltage at carrier frequency with only the carrier applied (signal voltage = 0).

Carrier null is achieved by balancing the currents in the differential amplifier by means of a bias trim potentiometer (R1 of Figure 5).

Carrier Suppression

Carrier suppression is defined as the ratio of each sideband output to carrier output for the carrier and signal voltage levels specified.

Carrier suppression is very dependent on carrier input level, as shown in Figure 22. A low value of the carrier does not fully switch the upper switching devices, and results in lower signal gain, hence lower carrier suppression. A higher than optimum carrier level results in unnecessary device and circuit carrier feedthrough, which again degenerates the suppression figure. The MC1496 has been characterized with a 60 mVrms sinewave carrier input signal. This level provides optimum carrier suppression at carrier frequencies in the vicinity of 500 kHz, and is generally recommended for balanced modulator applications.

Carrier feedthrough is independent of signal level, V_S. Thus carrier suppression can be maximized by operating with large signal levels. However, a linear operating mode must be maintained in the signal–input transistor pair – or harmonics of the modulating signal will be generated and appear in the device output as spurious sidebands of the suppressed carrier. This requirement places an upper limit on input–signal amplitude (see Figure 20). Note also that an optimum carrier level is recommended in Figure 22 for good carrier suppression and minimum spurious sideband generation.

At higher frequencies circuit layout is very important in order to minimize carrier feedthrough. Shielding may be necessary in order to prevent capacitive coupling between the carrier input leads and the output leads.

Signal Gain and Maximum Input Level

Signal gain (single–ended) at low frequencies is defined as the voltage gain,

$$A_{VS} = \frac{V_o}{V_S} = \frac{R_L}{R_e + 2r_e}$$
 where $r_e = \frac{26 \text{ mV}}{15(\text{mA})}$

A constant dc potential is applied to the carrier input terminals to fully switch two of the upper transistors "on" and two transistors "off" (V_C = 0.5 Vdc). This in effect forms a cascode differential amplifier.

Linear operation requires that the signal input be below a critical value determined by R_E and the bias current I5.

$$V_{S} \leq I5 R_{E}$$
 (Volts peak)

Note that in the test circuit of Figure 10, V_S corresponds to a maximum value of 1.0 V peak.

Common Mode Swing

The common-mode swing is the voltage which may be applied to both bases of the signal differential amplifier, without saturating the current sources or without saturating the differential amplifier itself by swinging it into the upper switching devices. This swing is variable depending on the particular circuit and biasing conditions chosen.

Power Dissipation

Power dissipation, P_D, within the integrated circuit package should be calculated as the summation of the voltage–current products at each port, i.e. assuming V12 = V6, I5 = I6 = I12 and ignoring base current, P_D = 2 I5 (V6 - V14) + I5) V5 - V14 where subscripts refer to pin numbers.

Design Equations

The following is a partial list of design equations needed to operate the circuit with other supply voltages and input conditions.

A. Operating Current

The internal bias currents are set by the conditions at Pin 5. Assume:

$$I5 = I6 = I12$$
,
 $IB < < IC$ for all transistors

then :

$$R5 = \frac{V - -\phi}{I5} - 500 \ \Omega$$
 where: R5 is the resistor between
Pin 5 and ground
 $\phi = 0.75 \text{ at } T_A = +25^{\circ}C$

The MC1496 has been characterized for the condition $I_5 = 1.0$ mA and is the generally recommended value.

B. Common–Mode Quiescent Output Voltage

V

Biasing

The MC1496 requires three dc bias voltage levels which must be set externally. Guidelines for setting up these three levels include maintaining at least 2.0 V collector–base bias on all transistors while not exceeding the voltages given in the absolute maximum rating table;

$$\begin{array}{l} 30 \; \text{Vdc} \; \geq \; [(\text{V6}, \text{V12}) - (\text{V8}, \text{V10})] \geq 2 \; \text{Vdc} \\ 30 \; \text{Vdc} \; \geq \; [(\text{V8}, \text{V10}) - (\text{V1}, \text{V4})] \geq 2.7 \; \text{Vdc} \\ 30 \; \text{Vdc} \; \geq \; [(\text{V1}, \text{V4}) - (\text{V5})] \geq 2.7 \; \text{Vdc} \end{array}$$

The foregoing conditions are based on the following approximations:

Bias currents flowing into Pins 1, 4, 8 and 10 are transistor base currents and can normally be neglected if external bias dividers are designed to carry 1.0 mA or more.

Transadmittance Bandwidth

Carrier transadmittance bandwidth is the 3.0 dB bandwidth of the device forward transadmittance as defined by:

$$\gamma_{21C} = \frac{i_0 \text{ (each sideband)}}{v_s \text{ (signal)}} \quad V_0 = 0$$

Signal transadmittance bandwidth is the 3.0 dB bandwidth of the device forward transadmittance as defined by:

$$\gamma_{21S} = \frac{i_0 \text{ (signal)}}{v_s \text{ (signal)}} \quad V_c = 0.5 \text{ Vdc}, \quad V_o = 0.5 \text{ Vdc}$$

Coupling and Bypass Capacitors

Capacitors C1 and C2 (Figure 5) should be selected for a reactance of less than 5.0 Ω at the carrier frequency.

Output Signal

The output signal is taken from Pins 6 and 12 either balanced or single-ended. Figure 11 shows the output levels of each of the two output sidebands resulting from variations in both the carrier and modulating signal inputs with a single-ended output connection.

Negative Supply

 $V_{\mbox{\scriptsize EE}}$ should be dc only. The insertion of an RF choke in series with $V_{\mbox{\scriptsize EE}}$ can enhance the stability of the internal current sources.

Signal Port Stability

Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source-tuned circuits that cause the oscillation.



An alternate method for low–frequency applications is to insert a 1.0 k Ω resistor in series with the input (Pins 1, 4). In this case input current drift may cause serious degradation of carrier suppression.



TEST CIRCUITS

Figure 6. Input–Output Impedance



NOTE: Shielding of input and output leads may be needed to properly perform these tests.





Figure 8. Transconductance Bandwidth









TYPICAL CHARACTERISTICS

Typical characteristics were obtained with circuit shown in Figure 5, $f_C = 500$ kHz (sine wave), V_C = 60 mVrms, $f_S = 1.0$ kHz, V_S = 300 mVrms, $T_A = 25^{\circ}$ C, unless otherwise noted.



Figure 13. Signal–Port Parallel–Equivalent Input Capacitance versus Frequency



Figure 12. Signal–Port Parallel–Equivalent Input Resistance versus Frequency



Figure 14. Single–Ended Output Impedance versus Frequency



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TYPICAL CHARACTERISTICS (continued)

Typical characteristics were obtained with circuit shown in Figure 5, f_C = 500 kHz (sine wave), V_C = 60 mVrms, f_S = 1.0 kHz, V_S = 300 mVrms, T_A = 25°C, unless otherwise noted.



VS, INPUT SIGNAL AMPLITUDE (mVrms)

f_C, CARRIER FREQUENCY (MHz)



OPERATIONS INFORMATION

The MC1496, a monolithic balanced modulator circuit, is shown in Figure 23.

This circuit consists of an upper quad differential amplifier driven by a standard differential amplifier with dual current sources. The output collectors are cross–coupled so that full–wave balanced multiplication of the two input voltages occurs. That is, the output signal is a constant times the product of the two input signals.

Mathematical analysis of linear ac signal multiplication indicates that the output spectrum will consist of only the sum and difference of the two input frequencies. Thus, the device may be used as a balanced modulator, doubly balanced mixer, product detector, frequency doubler, and other applications requiring these particular output signal characteristics.

The lower differential amplifier has its emitters connected to the package pins so that an external emitter resistance may be used. Also, external load resistors are employed at the device output.

Signal Levels

The upper quad differential amplifier may be operated either in a linear or a saturated mode. The lower differential amplifier is operated in a linear mode for most applications.

For low-level operation at both input ports, the output signal will contain sum and difference frequency components

and have an amplitude which is a function of the product of the input signal amplitudes.

For high–level operation at the carrier input port and linear operation at the modulating signal port, the output signal will contain sum and difference frequency components of the modulating signal frequency and the fundamental and odd harmonics of the carrier frequency. The output amplitude will be a constant times the modulating signal amplitude. Any amplitude variations in the carrier signal will not appear in the output.

The linear signal handling capabilities of a differential amplifier are well defined. With no emitter degeneration, the maximum input voltage for linear operation is approximately 25 mV peak. Since the upper differential amplifier has its emitters internally connected, this voltage applies to the carrier input port for all conditions.

Since the lower differential amplifier has provisions for an external emitter resistance, its linear signal handling range may be adjusted by the user. The maximum input voltage for linear operation may be approximated from the following expression:

$V = (I5) (R_E)$ volts peak.

This expression may be used to compute the minimum value of R_E for a given input voltage amplitude.



Figure 24. Typical Modulator Circuit



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Carrier Input Signal (V _C)	Approximate Voltage Gain	Output Signal Frequency(s)	
Low-level dc	$\frac{R_{L} V_{C}}{2(R_{E} + 2r_{e}) \left(\frac{KT}{q}\right)}$	fM	
High–level dc	$\frac{R_{L}}{R_{E}+2r_{e}}$	fM	
Low-level ac	$\frac{R_{L} V_{C}(rms)}{2\sqrt{2} \left(\frac{KT}{q}\right) (R_{E} + 2r_{e})}$	$f_{C} \pm f_{M}$	
High-level ac	$\frac{0.637 \text{ R}_{\text{L}}}{\text{R}_{\text{E}} + 2r_{\text{e}}}$	$f_C\pm f_M,\ 3f_C\pm f_M,\ 5f_C\pm f_M,\ .\ .\ .$	

Figure 25. Voltage Gain and Output Frequencies

 $\textbf{NOTES: 1. Low-level Modulating Signal, V_M, assumed in all cases. V_C is Carrier Input Voltage.}$

 When the output signal contains multiple frequencies, the gain expression given is for the output amplitude of each of the two desired outputs, f_C + f_M and f_C - f_M.

3. All gain expressions are for a single-ended output. For a differential output connection, multiply each

expression by two.

4. RL = Load resistance.

5. R_{E}^{-} = Emitter resistance between Pins 2 and 3.

6. $r_e =$ Transistor dynamic emitter resistance, at 25°C;

$$e \approx \frac{26 \text{ mV}}{\text{I}_5 \text{ (mA)}}$$

7. K = Boltzmann's Constant, T = temperature in degrees Kelvin, q = the charge on an electron.

 $\frac{\text{KT}}{\text{q}} \approx 26 \text{ mV}$ at room temperature

The gain from the modulating signal input port to the output is the MC1496 gain parameter which is most often of interest to the designer. This gain has significance only when the lower differential amplifier is operated in a linear mode, but this includes most applications of the device.

As previously mentioned, the upper quad differential amplifier may be operated either in a linear or a saturated mode. Approximate gain expressions have been developed for the MC1496 for a low–level modulating signal input and the following carrier input conditions:

- 1) Low-level dc
- 2) High-level dc
- 3) Low-level ac
- 4) High-level ac

These gains are summarized in Figure 25, along with the frequency components contained in the output signal.

APPLICATIONS INFORMATION

Double sideband suppressed carrier modulation is the basic application of the MC1496. The suggested circuit for this application is shown on the front page of this data sheet.

In some applications, it may be necessary to operate the MC1496 with a single dc supply voltage instead of dual supplies. Figure 26 shows a balanced modulator designed for operation with a single 12 Vdc supply. Performance of this circuit is similar to that of the dual supply modulator.

AM Modulator

The circuit shown in Figure 27 may be used as an amplitude modulator with a minor modification.

All that is required to shift from suppressed carrier to AM operation is to adjust the carrier null potentiometer for the proper amount of carrier insertion in the output signal.

However, the suppressed carrier null circuitry as shown in Figure 27 does not have sufficient adjustment range. Therefore, the modulator may be modified for AM operation by changing two resistor values in the null circuit as shown in Figure 28.

Product Detector

The MC1496 makes an excellent SSB product detector (see Figure 29).

This product detector has a sensitivity of 3.0 microvolts and a dynamic range of 90 dB when operating at an intermediate frequency of 9.0 MHz.

The detector is broadband for the entire high frequency range. For operation at very low intermediate frequencies down to 50 kHz the 0.1 μ F capacitors on Pins 8 and 10 should be increased to 1.0 μ F. Also, the output filter at Pin 12 can be tailored to a specific intermediate frequency and audio amplifier input impedance.

As in all applications of the MC1496, the emitter resistance between Pins 2 and 3 may be increased or decreased to adjust circuit gain, sensitivity, and dynamic range.

This circuit may also be used as an AM detector by introducing carrier signal at the carrier input and an AM signal at the SSB input.

The carrier signal may be derived from the intermediate frequency signal or generated locally. The carrier signal may be introduced with or without modulation, provided its level is sufficiently high to saturate the upper quad differential amplifier. If the carrier signal is modulated, a 300 mVrms input level is recommended.

Doubly Balanced Mixer

The MC1496 may be used as a doubly balanced mixer with either broadband or tuned narrow band input and output networks.

The local oscillator signal is introduced at the carrier input port with a recommended amplitude of 100 mVrms.

Figure 30 shows a mixer with a broadband input and a tuned output.

Frequency Doubler

The MC1496 will operate as a frequency doubler by introducing the same frequency at both input ports.

Figure 26. Balanced Modulator (12 Vdc Single Supply) Figures 31 and 32 show a broadband frequency doubler and a tuned output very high frequency (VHF) doubler, respectively.

Phase Detection and FM Detection

The MC1496 will function as a phase detector. High–level input signals are introduced at both inputs. When both inputs are at the same frequency the MC1496 will deliver an output which is a function of the phase difference between the two input signals.

An FM detector may be constructed by using the phase detector principle. A tuned circuit is added at one of the inputs to cause the two input signals to vary in phase as a function of frequency. The MC1496 will then provide an output which is a function of the input signal frequency.

TYPICAL APPLICATIONS

Figure 27. Balanced Modulator–Demodulator



Figure 28. AM Modulator Circuit

Figure 29. Product Detector (12 Vdc Single Supply)



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